Diplomarbeit

Design and Simulation of a Mixed Signal Testchip in a 0.35µm HV-CMOS Technology for High Precision DC Measurements

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Danksagung

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Kurzfassung

In der Halbleiterindustrie sind hochpräzise Simulationsmodelle unabkömmlich. Dafür müssen die zu modellierenden Halbleiterbauteile sehr genau charakterisiert werden. Weiters müssen die Unterschiede aller wesentlichen elektrischen Grössen von Bauteilen gleichen Layouts extrahiert werden.
Im Allgemeinen werden für statistische Analysen grosse Teststrukturen benötigt, welche mit einem enormer Messaufwand verbunden sind. Diese Arbeit beschäftigt sich mit dem Entwurf eines Testchips für hochgenaue DC-Charakterisierungen. Dazu wurde ein verbessertes Konzept entwickelt, welches eine schnelle und trotzdem hochpräzise Messung erlaubt. Für die automatische Messung der grossen Anzahl an Bauteilen wird eine serielle Adressierung verwendet. Eine der wichtigsten Komponenten der Teststruktur ist ein präzises hochspannungsfähiges Übertragungsglied, welches für die Selektion der einzelnen Elemente erforderlich ist. Weiters wurde ein Messgerät entwickelt, welches die Signale zur Steuerung des Testchips bereitstellt. Für die automatisierte Messung wurde ein spezielles Messprogramm geschrieben.
Hergestellt wird der Chips mittels 0.35μm Hochvolt - CMOS Technologie. Zusätzlich wurden Messungen am Übertragungsglied durchgeführt bzw. die elektrischen Eigenschaften der Bauelemente verifiziert. Die Ergebnisse der Simulation zeigen eine sehr gute Übereinstimmung mit den gemessenen Daten.

Abstract

In semiconductor industry highly precise simulation models are indispensable for circuit design. Therefore semiconductor devices have to be characterized on wafer accurately for SPICE modeling. Additionally variations of all significant properties of electronic components with identical layout have to be extracted for mismatch modeling.
Generally large test structures and an enormous effort for measurements are needed to acquire data for statistical analysis. In this thesis the design of a novel mixed signal test-chip is introduced for high precision DC measurements. An improved concept of measurement has been developed, where many devices can be measured fast and accurately. Serial addressing is used for automatic measurement of a large number of high voltage MOS transistor devices. The most important component of the circuit is a compact and highly accurate high voltage transmission gate which is needed for the selection of the device under test. Additionally, the measurement hardware which delivers signals to control the test-chip and a software for automatic measurements are provided.
The chip is manufactured using a 0.35 μm high voltage CMOS technology. Measurements are performed on the high voltage transmission gate and the characteristics of the devices under test are verified. The result of circuit simulation shows very good agreement with the measurement data.

Contents

List of Figures

List of Tables

List of Symbols

C	capacitance
$CGXO$	overlap capacitance
C_i	intrinsic gate-bulk capacitance
C_j	parasitic capacitance
C_{ox}	capacitance of the oxide
ϵ_0	permittivity of free space
ϵ_{ox}	permittivity of SiO_2
I_D	drain current
I_G	gate current
I_{leak}	leakage current
K	current gain factor
k_{ox}	dielectric constant of the insulator
λ	channel length modulation parameter
L	channel length
L_{eff}	effective channel length
LD	amount of overlap
n	electron concentration
nsq	number of squares
p	hole concentration
R	resistance
r_d	contact resistance of the drain
r_s	contact resistance of the source
r_{ds}	channel resistance
R_{field}	field resistance
R_{LOAD}	load resistance
R_{ON}	ON-resistance of the drain-source-channel
R_{OFF}	OFF-resistance of the drain-source-channel
t_{ox}	thickness of the oxide
μ_0	surface mobility of the channel (NMOS/PMOS)
V_A	Early voltage
V_B	bulk voltage
V_{BS}	bulk-source voltage
V_c	control voltage
V_{CE}	collector-emitter voltage
V_{CS}	collector-source voltage
V_D	drain voltage
V_{DB}	drain-bulk voltage
V_{DD}	positive supply voltage
V_{DS}	drain-source voltage

V_{EB}	emitter-basis voltage
V_G	gate voltage
V_{GB}	gate-bulk voltage
V_{GS}	gate-source voltage
V_{in}	input voltage
V_{out}	output voltage
V_{OS}	offset voltage
V_{pn}	diffusion voltage of a pn-junction
V_S	source voltage
V_{SS}	negative supply voltage
V_{th}	threshold voltage
V_{T0}	extrapolated threshold voltage
W	channel width
W_{eff}	effective channel width

List of Abbreviations

ADC	Analog Digital Converter
DC	Direct Current
$DEVAN$	Device Analysis software
DUT	Device Under Test
$DNTUB$	High Voltage Deep N-tub Layer
$GPIB$	General Purpose Interface Bus
$GNDU$	Ground Unit
HR	High Resolution
HV	High Voltage
LU	Logic Unit
MPW	Multi Product Wafer
$NMOSI$	Isolated Thin-Oxide NMOS
$NMOSI50T$	Isolated Thin-Oxide High-Voltage NMOS
OPA	Operational Amplifier
OS	Operating System
PA	Parameter Analyzer
$PJFET$	Pinched Retrograde P-tub Resistor
$PMOSI$	Isolated Thin-oxide PMOS
$PMOSI50T$	Isolated Thin-oxide High-Voltage PMOS
$PSUB$	P-substrate
$RDIFFNR$	Isolated N-Diffusion Resistor
$RDIFFPS$	P-Diffusion Resistor
$RNWELLS$	N-tub Resistor
$RPWELLR$	P-tub Resistor
SiO_2	Silicon Dioxide
SL	Scribe Line
SMD	Switch Mainframe Device
SMU	Source Monitor Unit
$V53$	Supply Voltage (53V)
$VERTN1$	Vertical npn (emitter=ndiff, basis=ptub, collector=dntub)
$VERTPH$	Vertical pnp (emitter=ptub, basis=dntub, collector=substrate)
WP	Worst Power
WS	Worst Speed

Chapter 1

Motivation

In semiconductor industry highly precise simulation models are indispensable for circuit design. Therefore semiconductor devices have to be characterized on wafer accurately for SPICE modeling. Additionally variations of all significant properties of electronic components with identical layout have to be extracted for mismatch modeling. In integrated circuits MISMATCH limits the performance of analog and especially mixed signal circuits. Some applications need devices which are required to match. Examples are differential input stages or a chain of resistors operating as a voltage reference in a ADC. Especially long-distance mismatch is a very important effect which has to be characterized and investigated accurately. The reasons for distance mismatch are mainly process gradients across the wafer. Further, pair mismatch is a statistical effect depending on dopant density fluctuation. All these influences can be measured and the gained parameters can be used for circuit simulators or design guidelines.

The idea is to develop a matrix test chip which consists of different types of high voltage MOSFET devices with different geometry for automated analysis. There is the possibility to characterize short distance, long distance and also pair mismatch. This new design will become a considerable step forward for the characterization itself. The measurement principle is illustrated in Fig. 1.1.

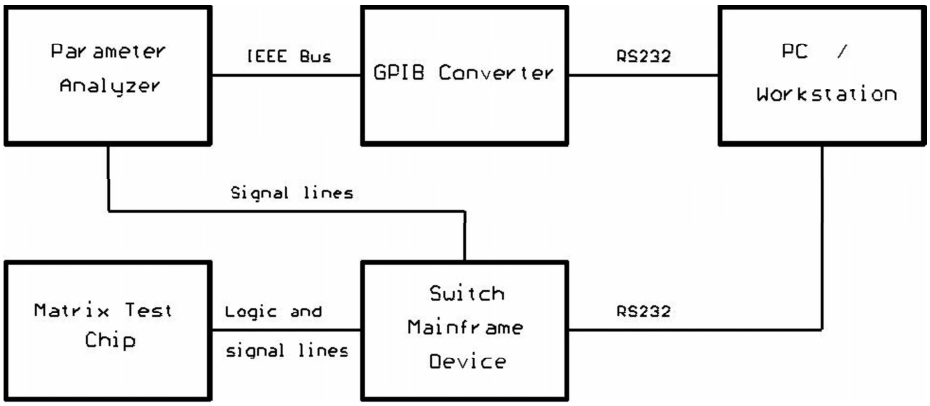

Figure 1.1: Principle of the automated device measurement

Therefore the matrix test chip is connected with a special designed probe card to place it in a 'Cascade Microtech' prober. A special developed switch mainframe device (SMD) includes a control logic for device selection of the test macro. The SMD can be controlled via a front panel or via a PC / Workstation for automated measurements. The OS independent software writes the settings to the PA and reads/stores the data in a convenient format when measurement has finished. Then this file can be consulted for DC characterization and parameter extraction. To enable a communication between computer and PA a high-performance serial-to-GPIB interface is required. See chapter 3 for details.

1.1 Measurement principle

The measurement principle uses a four-terminal method with regulated reference potential to avoid parasitic resistance effects which would decrease the precision of measurements. For this potential regulation so-called force-source signals are used. Fig. 1.2 illustrates the error compensation.

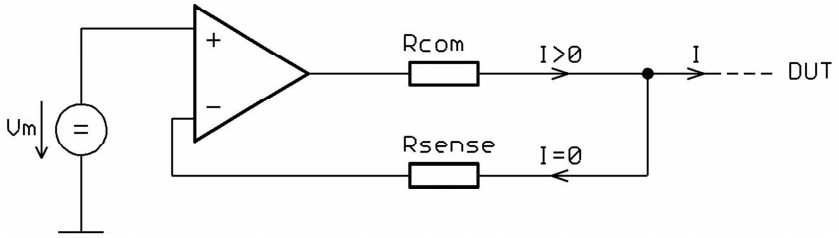

Figure 1.2: Potential regulation with the force/sense method

The adjusted voltage *Vm* forces a current through the device under test (DUT). This current causes a voltage drop on the series resistance *Rcom*. Without using a force/sense method the voltage drop leads to an error which depends on the value of the parasitic resistance and the forced current. By using a sense path the operational amplifier (OPA) minimizes the differential voltage to zero so that the voltage at the DUT is exactly the input voltage *Vm*. The current in the sense path is nearly zero because of the high impedance of the OPA input stage. When measuring a device the sense lines should be connected to the device as close as possible to increase the accuracy. In addition, a particular attention has to be directed to leakage currents which could not be compensated with the four-terminal method.

Chapter 2

Design of the Matrix Test Chip

This chapter deals with the gradually design of the matrix test chip. First the concept and the structure of the chip are described. Then the specifications and the available circuit devices are briefly summarized. Since the a high precision analog switch is the heart of the design, the MOS transistor and its most important applications like switches, transmission-gates and current sources are investigated in detail. Then the considerations for the special high voltage switches are summarized and the comparison of measurement data and simulation is shown.

2.1 Structure of the test chip

First the structure of the test chip had to be determined. Here a matrix structure will be an optimum for the placement of the devices to be investigated. Additionally, this design allows the characterization of devices with the same layout either in line or across the test macro. Further, there is the advantage of addressing to minimize the control lines. Fig. 2.1 shows basically the structure of the chip with its main parts.

The logical unit (LU) consists of two shift register blocks which allow to address each device individually. For that the LU uses three signals, one clock signal to increase the vertical index, one clock signal to increase the horizontal index and one for reset of the logic blocks. To switch the parameter analyzer (PA) signals as accurate as possible to the devices special low scaled analog switches are necessary. The addressing of the test structure is applied externally.

2.2 Specifications

Before designing the test chip some specifications have to be taken into account. To be adaptable these considerations had to be done carefully to avoid unwanted costly redesigns.

Operating voltages V_{GS} on the gate of the test device:

- 0 to 3.6 V for 7nm oxide thickness
- 0 to 5.5 V for 14nm oxide thickness

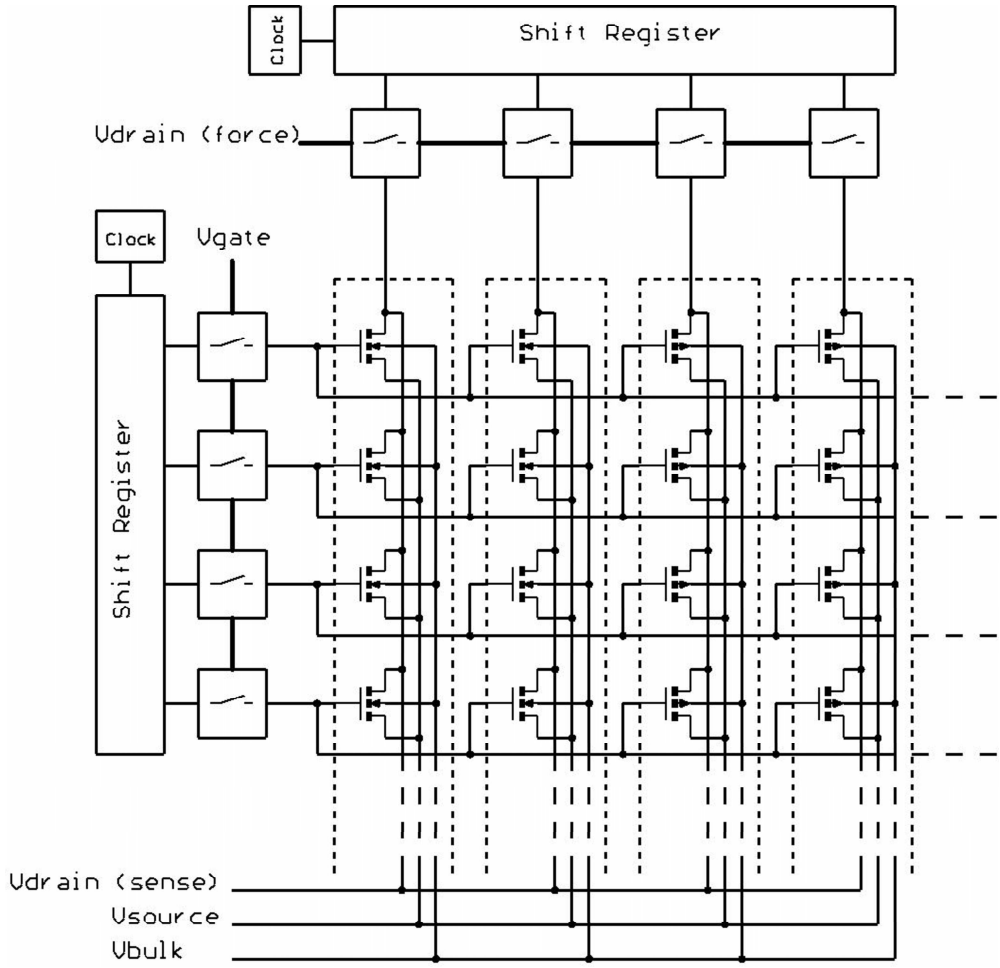

Figure 2.1: Structure of the matrix test chip

- 0 to 20 V for 50nm oxide thickness

Operating voltages V_{DS} on the drain of the test device:

- 0 to 50 V

Operating voltages V_{BS} on the bulk of the test device:

- 0 to -3.6 V

2.3 Available Circuit Elements

To be adaptable and more flexible to the production process only few types of devices were used for the mixed signal test chip. There are several process modules based on the core process which have different number of masks. Also they are different in their module capability. Reducing the number of masks goes equal with reducing

costs. Additionally, test macros with different device structures should be placeable on any multi product wafer (MPW). Therefore, only devices were applied which can be produced with a minimum of mask numbers.

Here is the list of possible devices:

- MOSFETS:

  nmosi: isolated thin-oxide nmos
  nmosi50t: isolated thin-oxide high-voltage nmos
  pmosi: isolated thin-oxide pmos
  pmos50t: thin-oxide high-voltage pmos

- RESISTORS:

  rdiffnr: isolated n-diffusion resistor
  rdiffps: p-diffusion resistor
  rnwells: n-tub resistor
  rpwellr: p-tub resistor
  pjfet: pinched retrograde p-tub resistor

- BIPLOARS:

  vertn1: vertical npn (emitter=ndiff, basis=ptub, collector=dntub)
  vertph: vertical pnp (emitter=ptub, basis=dntub, collector=substrate)

The next step is to develop analog sub circuits. Then these circuits will be combined with other simple circuits to generate a more complex circuit function. Consequently, the declaration of the next circuits can be considered as building blocks.

2.4 MOSFET Switch

One of the most used circuits in integrated designs is the MOSFET switch which can be found in numerous applications. It is used as a transmission gate in digital circuits, for modulation, multiplexing and in many other applications. To build a useful switch for the matrix test chip some studies have to be done. Two of the most important characteristics of a switch are the terminal resistance in the ON state (R_{ON}) and in the OFF state (R_{OFF}). Ideally $R_{OFF} \rightarrow \infty$ and $R_{ON} \rightarrow 0$. In addition there are also parasitic capacitances which have to be discussed. Fig. 2.3 illustrates an equivalent circuit diagram for a non ideal switch.

V_{OS} is the so called offset voltage that may exist when the switch is in the ON state and the current through the channel is not equal 0. The leakage current that may flow in the OFF state of the switch is modeled with the current source I_{OFF} and the resistor R_{OFF}. R_1 and R_2 consider the junction leakage currents of the source-bulk and drain-bulk junctions. C_{13} and C_{23} are overlap capacitances as shown in Fig. 2.2.

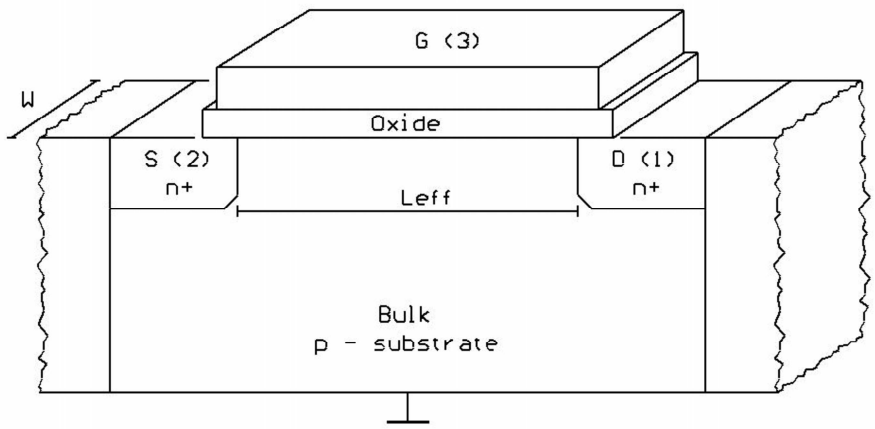

Figure 2.2: Structure of a n - channel MOS transistor

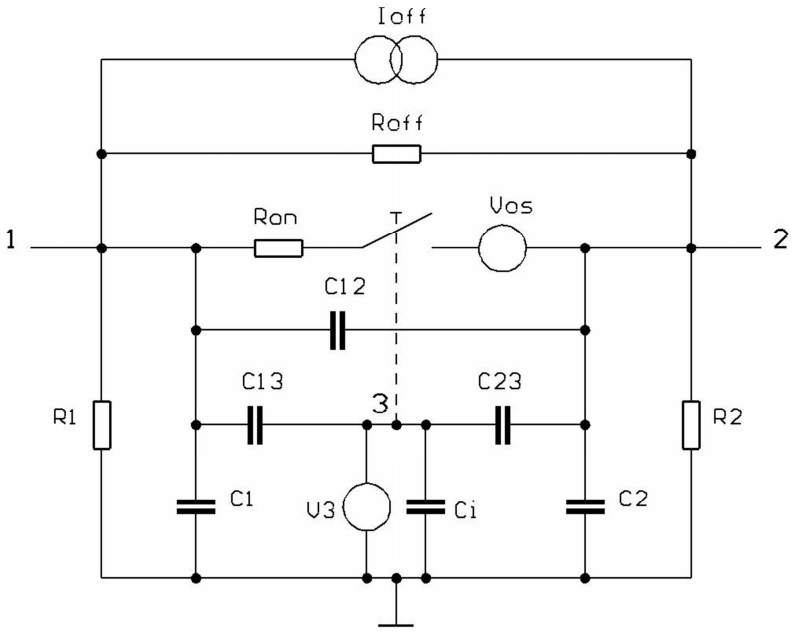

Figure 2.3: Equivalent circuit diagram for a non ideal switch, from [1]

They can be approximated as

$$C_{13} = C_{23} \cong (LD)(W_{eff})C_{ox} = (CGXO)W_{eff} \tag{2.1}$$

CGXO (X = S or D) ... overlap capacitance [F/m^2]
W_{eff} ..... channel width [m]
LD ..... amount of overlap [m]
C_{ox} ..... capacitance per unit area of the gate oxide [F/cm^2]

The most important capacitance, which actually limits the switching speed is the intrinsic gate-bulk capacitance C_i. It is approximated by

$$C_i = \frac{\epsilon_{ox}\ W_{eff}\ L_{eff}}{t_{ox}} \tag{2.2}$$

if the device is in accumulation or in the strong inversion operating regime. Additionally an overlap capacitance can be found between the gate and the bulk which is a function of the effective length of the channel, L_{eff}. C_1, C_2 and C_{12} are the drain - bulk, source - bulk and source - drain capacitance which are all depletion capacitances that vary with the voltage.

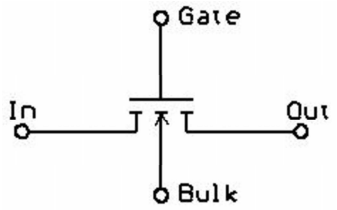

Figure 2.4: n - channel MOS transistor used as a switch

As shown in Fig. 2.4 you can use either the drain or the source as input or output of the switch. This is given if the MOS transistor is nearby symmetric.

A very appropriate model of a MOS device [1] is given by

$$I_D = \begin{cases} 0 & V_{GS} < V_{th} \\ K\ V_{DS}\ (V_{GS} - V_{th} - \frac{V_{DS}}{2})\ (1 + \lambda V_{DS}) & V_{GS} \geq V_{th},\ 0 \leq V_{DS} < V_{GS} - V_{th} \\ \frac{K}{2}\ (V_{GS} - V_{th})^2\ (1 + \lambda V_{DS}) & V_{GS} \geq V_{th},\ V_{DS} \geq V_{GS} - V_{th} \end{cases} \tag{2.3}$$

$$I_G = 0 \tag{2.4}$$

$$K = K' \frac{W_{eff}}{L_{eff}} = \mu_0\ C_{ox}\ \frac{W_{eff}}{L_{eff}} \tag{2.5}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}\ ,\ \epsilon_{ox} = k_{ox}\ \epsilon_0 \tag{2.6}$$

$$\lambda = \frac{1}{V_a} \tag{2.7}$$

Definition of the various parameters:

I_D	drain-source current
I_G	gate current
K	current gain factor
μ_0	surface mobility of the channel (NMOS or PMOS) [$cm^2/(Vs)$]
W_{eff}	effective channel width [μm]
L_{eff}	effective channel length [μm]
λ	channel length modulation parameter [1/V]
C_{ox}	capacitance per unit area of the gate oxide [F/cm^2]
C_i	intrinsic gate-bulk capacitance [F]
V_a	Early voltage [V]
ϵ_{ox}	permittivity of SiO_2 [F/cm]
ϵ_0	permittivity of free space (8.854 $aF/\mu m$)
k_{ox}	dielectric constant of the insulator; for $SiO_2 : k_{ox} = 3.9$
t_{ox}	thickness of the insulator [cm]

The following figures [1] illustrate the characteristics of a MOS device:

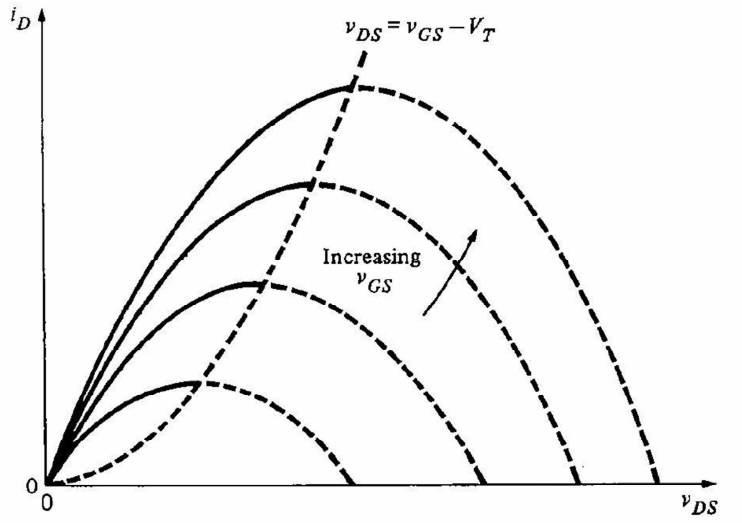

Figure 2.5: Graphical illustration of the Eq. (2)

In Fig. 2.5 I_D is plotted as a function of V_{DS} at different V_{GS} and $\lambda = 0$. With the increase of V_{GS} also the current increases proportionally. In the saturation region, where the saturation voltage is given as

$$V_{DSsat} = V_{GS} - V_{th} \tag{2.8}$$

the drain current reaches a maximum.

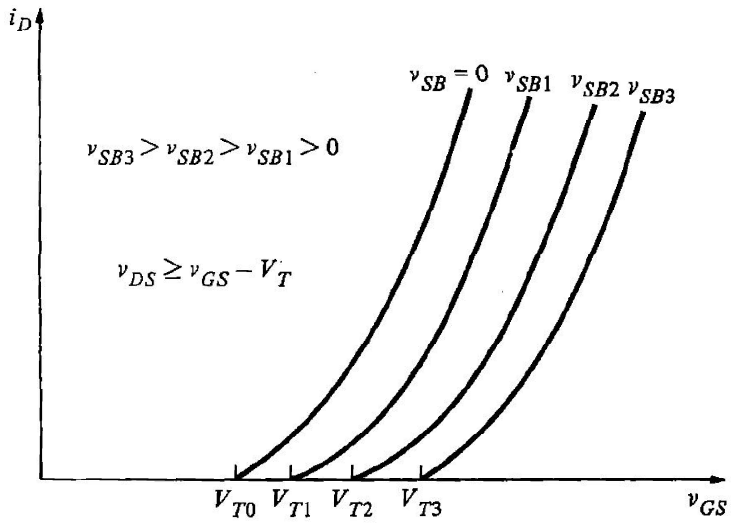

Figure 2.6: Transfer characteristics of a nMOS transistor depending on the source - bulk voltage

Fig. 2.7 shows the normalized output characteristic of the MOS transistor which also can be described by Eq. (2.3). In the cutoff region where $V_{GS} < V_{th}$ the current through the channel is 0. A small drain - source voltage ($V_{GS} - V_{th} < V_{DS}$) and an increasing gate - source voltage causes a current which lies between the I_D - axis and the $V_{GS} - V_{th} = V_{DS}$ curve (linear region). In the saturation region the MOS device is said to saturate and the drain current stays unchanged in case of $\lambda = 0$ ($V_a \rightarrow \infty$). For a nonzero Early voltage I_D is increasing slightly corresponding to the dashed lines of the curves.

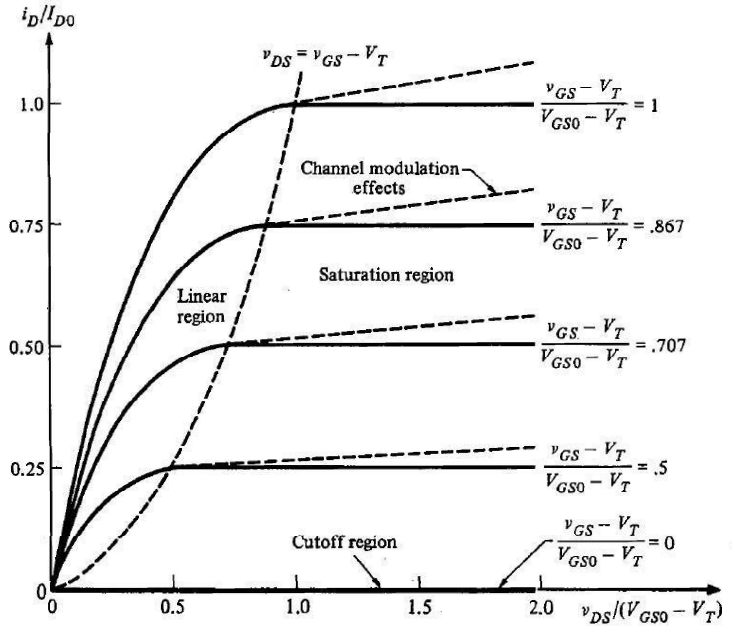

Figure 2.7: Normalized output characteristics of a MOS transistor

As shown in Fig. 2.6 the drain current is plotted as a function of the gate - source voltage. Very important is the dependency of the transfer function on the value of the

source-bulk voltage which is called *body effect*. The threshold voltage increases if positive V_{SB} is applied and minimum V_{th} can be found at zero source-bulk biasing. Very interesting is the fact that a n-channel depletion device can become an enhancement device. If V_{SB} is large enough, V_{th} will actually become positive.

2.4.1 The ON resistance

As mentioned above the channel resistance of a MOSFET is especially in the ON state a very important parameter. If the MOS switch is closed, the resistance is made up of the contact resistances of drain and source, r_s, r_d and the channel resistance r_{ds}. To illustrate the resistive behavior of a MOS switch the Eq. (2.3) can be consulted. Using the equation for the linear region, where $V_{GS} \geq V_{th}$, $0 \leq V_{DS} < V_{GS} - V_{th}$, with the parameters $W = L = 10\mu m$, $\epsilon_{ox} = 3.45 \cdot 10^{-6}\ F/cm^2$, $t_{ox} = 50\ nm$, $\mu_0 = 370\ cm^2/Vs$, $V_{th} = 1V and\ \lambda = 0.01\ V^{-1}$ yields the drain current shown in Fig. 2.8.

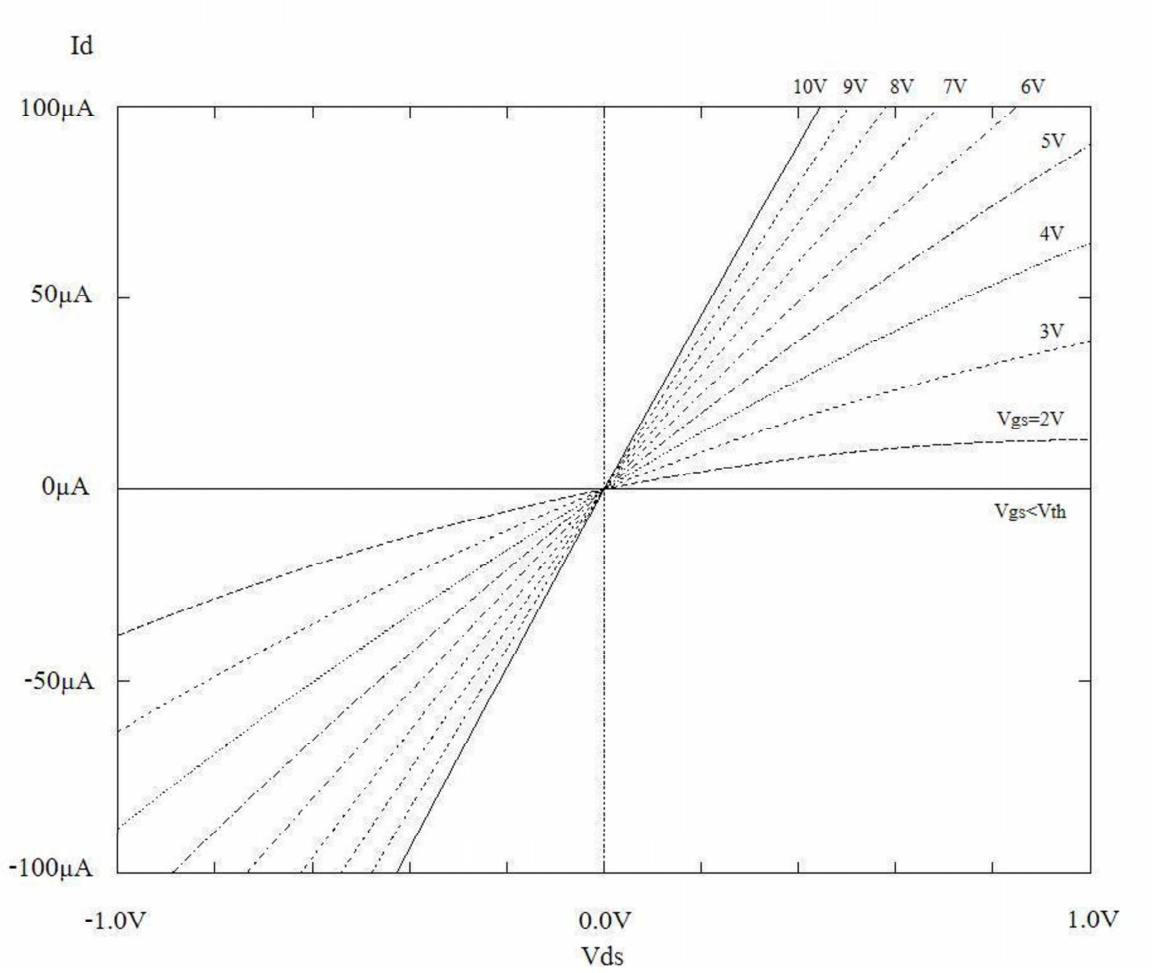

Figure 2.8: ON characteristic: I_D as a function V_{DS}, V_{GS} varied

If $V_{GS} < V_{th}$, the drain-source current is 0 and $R_{ON} \approx \infty$ (the MOS transistor is isolated). For V_{GS} beyond V_{th} the MOS device becomes conductive and the channel current increases. Additionally, for increasing V_{DS} the drain current begins to saturate and the curves will start to decrease in slope.

Ignoring the offset voltage of the MOS switch ($V_{OS} = 0$) the large-signal model from [1] can be used to calculate the resistance of the device in the ON state.

$$R_{ON} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{L}{\mu_0 C_{ox} W (V_{GS} - V_T)}, \ \lambda = 0 \tag{2.9}$$

As shown in Eq. (2.9) R_{ON} is a function of the gate-source voltage V_{GS}. As illustrated in Fig. 2.9 the ratio of W/L is very important. A small value of R_{ON} is achieved, if the device has a large channel width W and a short channel length L.

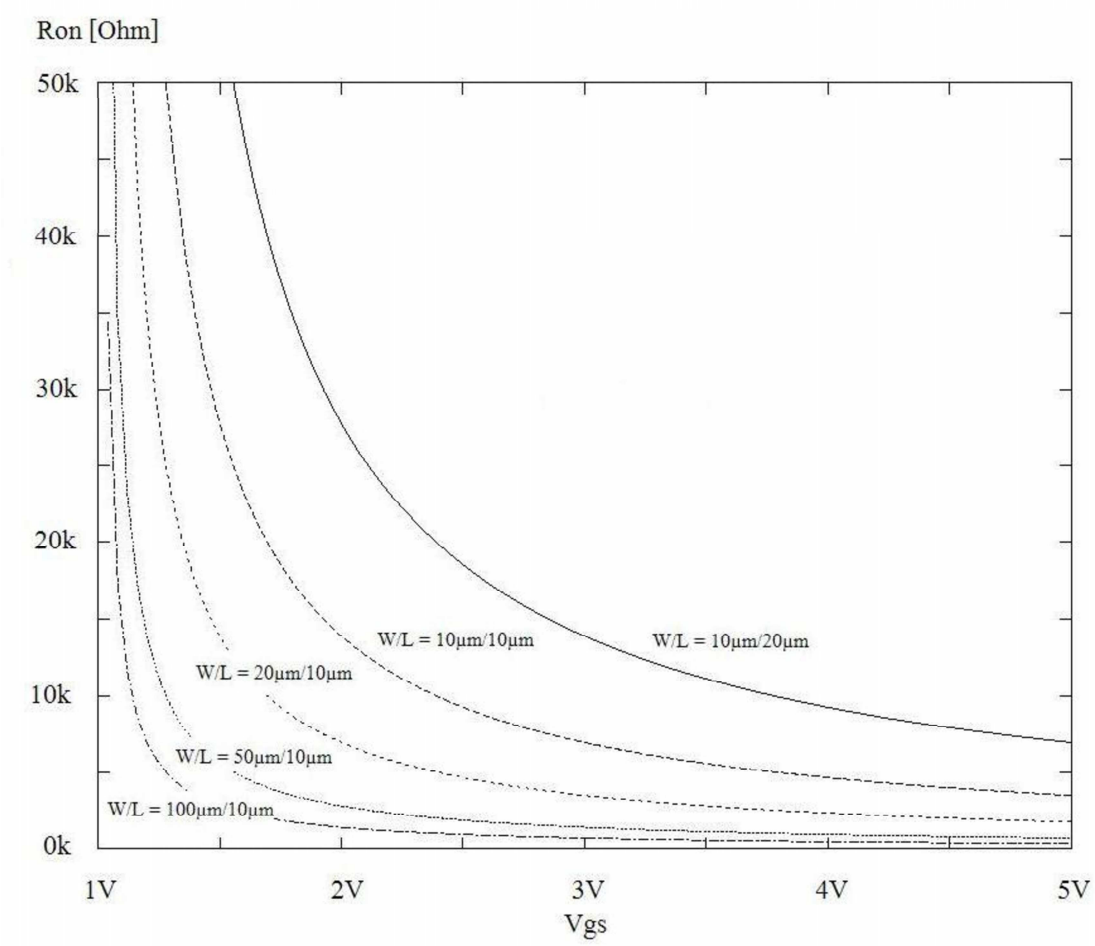

Figure 2.9: ON state resistance as a function of V_{GS}, W/L varied

The OFF state resistance R_{OFF} for $V_{GS} \leq V_{th}$ tends to ∞ for the ideal case, typical values are approximately $R_{OFF} = 10^{12}$ ohms. In many cases the leakage current of a MOS transistor, which can be combined of the sub-threshold current, the drain-bulk diode and source-bulk diode leakage currents, the package-leakage current and finally the surface-leakage current must be taken into account. A typical value is in the $I_{leak} = 10pA$ range at room temperature which doubles for every 8°C increase. This effect can be disastrous if a design contains capacitances which should not be charged via MOS switches which are opened due to high temperature.

2.4.2 Transmission Gate

The switch variant discussed above may not be practicable in some cases, if the ranges of the operating voltages are considered. Using a nMOS switch the transistor is only in the ON state if the input voltage (normally the voltage on the source) is smaller than the control voltage on the gate. Since the bulk of the nMOS is the substrate, the bulk potential V_- is always V_{SS}. An example is shown in Fig. 2.10.

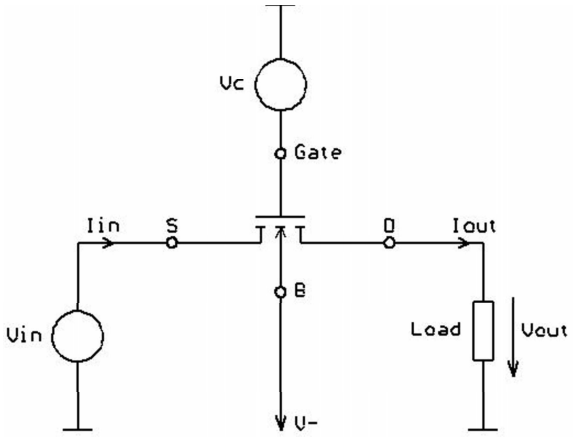

Figure 2.10: Application of a nMOS transistor used as a switch

Assuming V- = 0 and $V_c = 10$V, the voltage V_{in} on the switch terminal source should be in the range $0 \leq V_{in} < V_c - V_{th}$ to ensure that the nMOS transistor is ON. If the input voltage achieves the upper limit, then the switch begins to turn OFF. Additionally, one has to keep in mind, that V_{th} depends on the bulk-source voltage V_{BS}. It suggests itself to connect a p-channel MOS transistor in parallel to the nMOS. That gives the so called transmission gate which avoids many problems compared to a single-channel MOS switch.

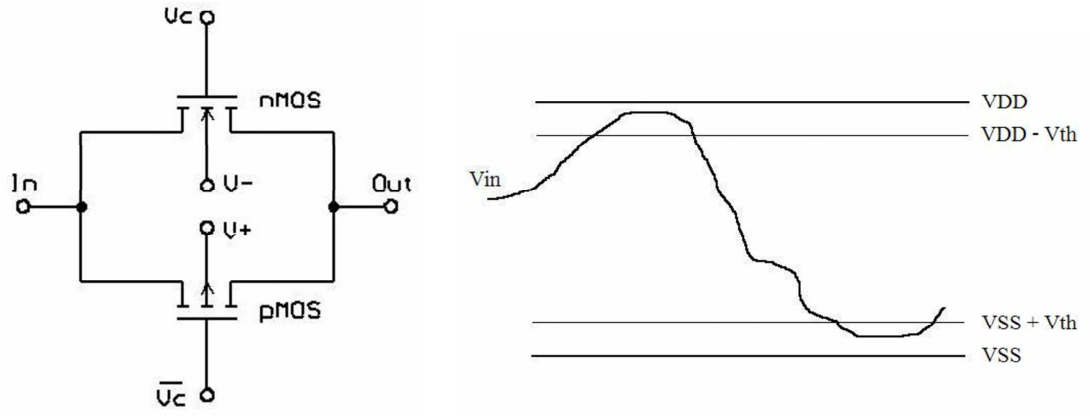

Figure 2.11: Transmission gate and the operating voltage range

The dynamic analog signal range is significantly increased compared to the single - channel switch. For high control bias V_c on the gate, both MOS devices are in the ON state. The transistors are working in parallel and so the combined resistance R_{ON} is smaller

than value of either. Typically the ON impedance can be lower than 1kΩ, especially if using transistors with a large W to L ratio. The input voltage V_{in} has to be between V_{DD} and V_{SS} as shown on the right hand side of Fig. 2.11. For the control voltage V_C we find $V_C = V_{DD}$ and $\overline{V_C} = V_{SS}$.

In Fig. 2.10 the source is connected to the input. Due to the symmetrical structure of a nMOS device the terminals are not determined until applying the voltages. The source of a nMOS transistor has normally a lower potential than the drain. In the ON state the output-signal will follow the input-signal, so that the voltage V_{out} is approximately equal but a little bit less than the input voltage V_{in}. The drain is connected to the input terminal. The voltage drop in the drain-source-channel depends on the current through the switch which is normally very low. So V_{DS} is low and the nMOS transistor operates in the linear region. The bulk of the nMOS is connected to the most negative potential of the circuit (here V_{SS}). In contrast to to nMOS device, the source of a pMOS transistor has a higher potential than the drain, which means that the source is the input terminal.

Here are the operating voltage ranges of each device in the ON state

$$\begin{aligned} nmos: &\quad V_{SS} \leq V_{in} \leq V_{DD} - V_{th_{nMOS}} \\ pmos: &\quad V_{SS} + \left|V_{th_{pMOS}}\right| \leq V_{in} \leq V_{DD} \end{aligned} \tag{2.10}$$

The combined parallel resistance can be summarized as follows:

$$\begin{aligned} R_{ON} = R_{ON_{nMOS}}: &\quad V_{SS} \leq V_{in} \leq V_{SS} + \left|V_{th_{pMOS}}\right| \\ R_{ON} = R_{ON_{nMOS}} \| R_{ON_{pMOS}}: &\quad V_{SS} + V_{th_{pMOS}} < V_{in} \leq V_{DD} - Vth_{nMOS} \\ R_{ON} = R_{ON_{pMOS}}: &\quad V_{DD} - Vth_{nMOS} < V_{in} \leq V_{DD} \end{aligned} \tag{2.11}$$

The W/L ratios of the nMOS device and the pMOS device are usually chosen to be the same. The nMOS transistor has a larger transconductance K than the pMOS device. This fact causes $R_{ON_{pMOS}} > R_{ON_{nMOS}}$ for the same effective V_{GS}. In Fig. 2.12 the ON resistance of the transmission gate is illustrated as a function of the terminal voltage difference between input and output. The bulk of the nMOS is connected to V_{SS} (0V), the bulk of the pMOS is biased to V_{DD}. The gates of the n-channel and p-channel devices are connected to V_{DD} and V_{SS}. As can be seen in the figure, in the middle of the resistance curve there is a peak which is caused by the different R_{ON} values of each MOS transistor. Additionally, the bulk-bias effect increases the threshold voltages resulting in a higher resistance.

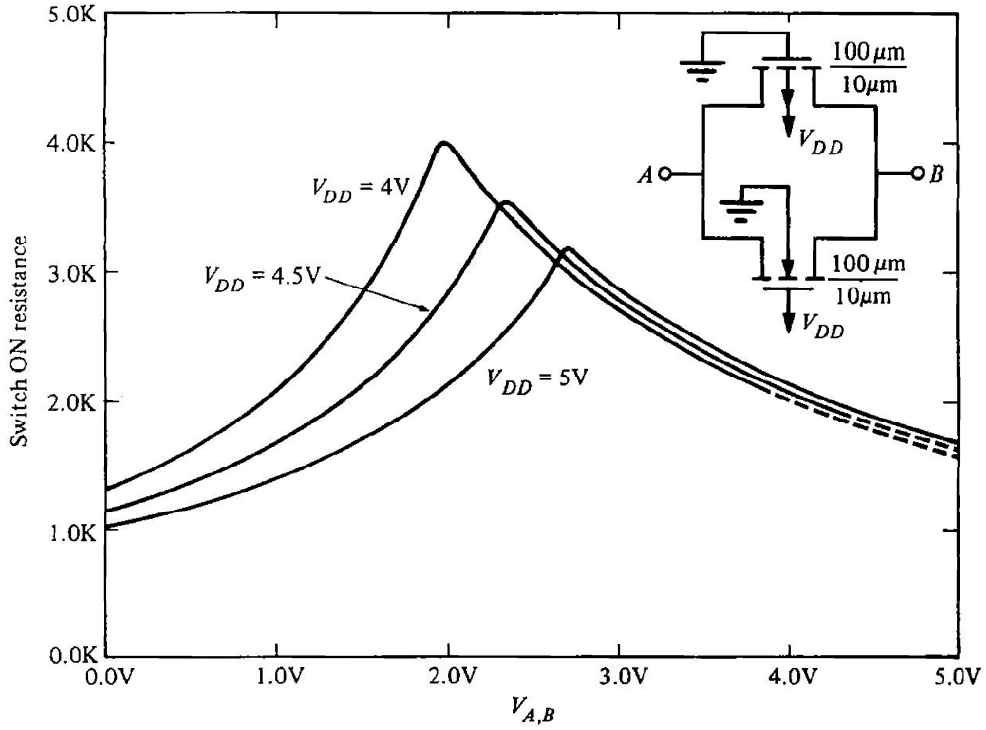

Figure 2.12: R_{ON} as a function of the terminal voltage difference V_{AB}, V_{DD} varied, from [1]

2.5 Analog switch design

As declared in the specifications 2.2 the maximum voltage on the gate of a test device is $V_{GS_{max}} = 20V$ (for 50nm oxide thickness), and the maximum voltage on the drain is $V_{DS_{max}} = 50V$. That implies that the control voltages on the gates of the n-channel and p-channel devices of a t-gate must be biased to $50V$ and $0V$. One problem is that there is no shift logic available to handle with such high potentials. On the other hand the large operating voltage ranges could destroy used elements if potentials are beyond the allowed operating conditions. The maximum operating voltage ratings of all elements available for the circuit design are shown below.

2.5.1 Operating conditions

Table 2.1: Ratings for isolated 3.3 Volt NMOS and PMOS transistors

NMOSI	V_{GS}	V_{DS}	V_{GB}	V_{DB}	V_{SB}	$V_{B-dntup}$	$V_{dntub-psub}$
[V]	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	-20 (-25)	50 (55)

PMOSI	V_{GS}	V_{DS}	V_{GB}	V_{DB}	V_{SB}	V_{B-psub}
[V]	-3.6 (-5)	-3.6 (-5)	-3.6 (-5)	-3.6 (-5)	-3.6 (-5)	50 (55)

Table 2.2: Ratings for high voltage NMOSI (isolated) and PMOS transistors with thin gate oxide

NMOSI50T	V_{GS}	V_{DS}	V_{GB}	$V_{SB-psub}$	V_{D-psub}
[V]	3.6 (5)	50 (55)	3.6 (5)	> 0	50 (55)

PMOS50T	V_{GS}	V_{DS}	V_{GB}	V_{D-psub}	V_{SB}	V_{B-psub}
[V]	-3.6 (-5)	-50 (-55)	-3.6 (-5)	$>$ -45	-3.6 (-5)	50 (55)

Table 2.3: Ratings for vertical NPN, PNP transistors and p-channel junction FET

VERTN1	V_{CE}	V_{EC}	V_{EB}	V_{CS}
[V]	10 (13)	2 (3)	9 (11)	50 (55)

VERTPH (C=S)	V_{CE}	V_{EC}	V_{EB}	V_{BS}
[V]	-55 (-70)	-	-45 (-60)	-

PJFET	$V_G - V_{SUB}$	V_{SG}	V_{DG}
[V]	50 (55)	-40 (-45)	-40 (-45)

Table 2.4: Ratings for available resistors

Resistors	Device-name	$V_{term-bulk}[V]$	$V_{bulk-substrate}[V]$
High voltage n-well	RNWELLS	50 (55)	-
n+ diffusion isolated	RDIFFNR	5.5 (7)	50 (55)
p+ diffusion isolated	RDIFFPS	-5.5 (-7)	50 (55)
p-well (in DNTUB)	RWELLR	-25 (-30)	50 (55)

Note: The values in brackets denote absolute maximum ratings at reduced lifetime.

Applying the required operating conditions to a convenient t-gate causes several problems with the maximum voltage ranges of the analog switch. Using the circuit in Fig. 2.13 with the MOS transistors NMOSI50T and PMOS50T the maximum peak values of V_{GS} of these n-channel and p-channel devices are 3.6V maximal (see Tab. 2.2). Assuming the input voltage of the switch is 20V (corresponding to the maximal V_{GS} of a test device) the output voltage should have the same potential in the ON state. The gate-source voltages V_{GS1} and V_{GS2} of the t-gate transistors should lie between the required threshold voltages and the maximum ratings of the gate-source voltages.

Threshold voltage (40x10 μm) : $NMOSI50T, PMOS50T$

$$\begin{aligned} NMOSI50T: \quad V_{th} &= 0.35Vmin \ \ldots \ 0.47Vtyp \ \ldots \ 0.59Vmax \\ PMOS50T: \quad -V_{th} &= 0.51Vmin \ \ldots \ 0.66Vtyp \ \ldots \ 0.81Vmax \end{aligned} \tag{2.12}$$

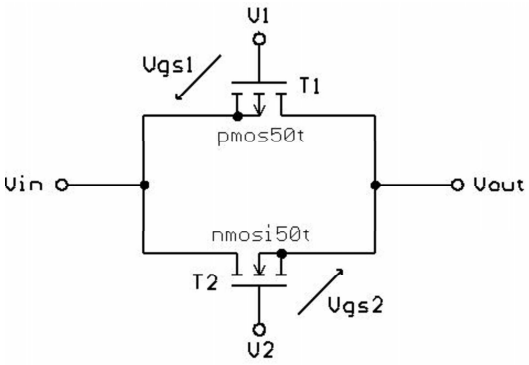

Figure 2.13: Transmission gate using available MOS devices

Table 2.5: Operating voltages of the t-gate (Fig. 2.13) in ON and OFF state

Switch	V_{in}	V_{out}	V_{GS1}	V_1
ON	0-20V	0-20V	-3.6V max	$V_{in} - 3.6V < V1 < V_{in} - \|V_{th1}\|$
OFF	0-20V	0V	0V	V_{in}

Switch	V_{in}	V_{out}	V_{GS2}	V_2
ON	0-20V	0-20V	3.6V max	$V_{in} + \|V_{th2}\| < V2 < V_{in} + 3.6V$
OFF	0-20V	0V	0V	0V

As shown in Tab. 2.5 the potential on the gates of the MOS transistors T1 and T2 must be between $V_{in} - 3.6V < V1 < V_{in} - |V_{th1}|$ and $V_{in} + |V_{th2}| < V2 < V_{in} + 3.6V$ in the ON state. It follows that the voltage levels provided by the digital control logic (shift register), normally 3.3 V, have to be shifted to higher values to guarantee that the devices are still conductive if high input voltages are applied. In the OFF state the gate voltage V_1 of the p-channel device must be equal to the input voltage to avoid a gate-source breakdown.

2.5.2 Level shifting

As mentioned above a level shifter is used to convert a low voltage control signal to a high voltage control signal. The following lines show a way to generate such signals. To reduce the space requirements of the test chip the circuit has to be kept as simple as possible. The first part of our level shifter is a current sink. It provides a current which is independent of the terminal voltage at any instant time. As described in [1]: The gate is raised to whatever voltage necessary to create the desired value of current. They note that in the linear region the MOS device is not a good current source. In fact the voltage across the current sink must be larger than V_{min} to guarantee that the current sink performs properly. As shown in Fig. 2.14 this means that

$$\nu_{out} \geq V_{GG} - V_{T0} - V_{SS} \tag{2.13}$$

If the gate-source voltage is held constant, the large-signal characteristic of the n-channel MOS transistor is given by the output characteristic of Fig. 2.7. If the source and bulk

are connected to V_{SS}, the small-signal output resistance is given by

$$r_{out} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D} \tag{2.14}$$

If source and bulk are not connected to the same potential, the characteristics will not change as long as V_{BS} is a constant. The voltage V_{min} can be influenced by the W/L ratio of the transistor and should be chosen as small as possible. Additionally, the parameter λ should be a minimum to minimize the influence of the terminal voltage V_{DS}.

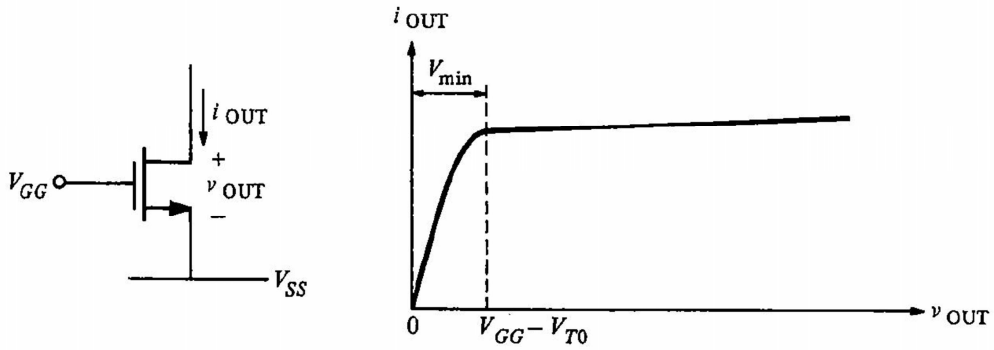

Figure 2.14: Current sink and its characteristics, from [1]

2.6 Design for n-channel MOS transistors

To generate a voltage drop a resistor has to be positioned between the drain port of the NMOS device and the positive node V_{DD}. As shown in Fig. 2.15 a resistance of a high voltage n-well is used in the circuit.

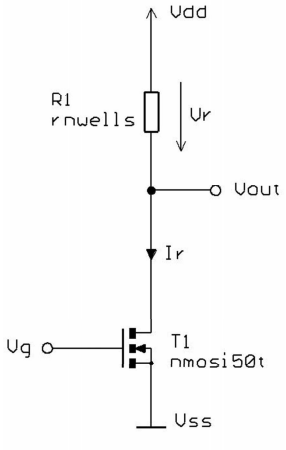

Figure 2.15: Current sink with load resistor RNWELLS

The typical n-well sheet resistance of the RNWELLS is 1.33 kΩ. The device rules claim a minimum width of 4 μm. Generally, the value of a resistance can be adjusted with the number of squares $nsq = L/W$ (design guideline minimum: $nsq_{min} = 5\square$).

Using a W/L ratio of 4/20 gives a resistance value

$$R_1 \approx \frac{L}{W_{eff}} R_{field} = \frac{20}{4.3} 1.33k\Omega/\square = 6.186k\Omega \tag{2.15}$$

Table 2.6: Used device parameters of the current source in Fig. 2.15

Device	Width $[\mu m]$	Length $[\mu m]$
nmosi50t	10	5
rnwells	4	20

The proper choice of the W/L ratio of the n-channel device is important for a good functioning of the current source, since V_{min} depends on W/L. Therefore, the device characteristics in the process documentation have to be studied to find the appropriate dimension values having a small V_{min} (see Fig. 2.14). Then the circuit can be simulated with *Cadence*. The control voltage V_g of the current sink is set to a common digital potential of 3.3 Volts. Now the voltage V_{out} can be shifted with the voltage V_{DD} assuming that $V_{DS_{T1}} > V_{min}$. This voltage drop can provide the gate-source voltage for the pMOS device of the t-gate (see Fig. 2.18). The following figures show the results of the simulation.

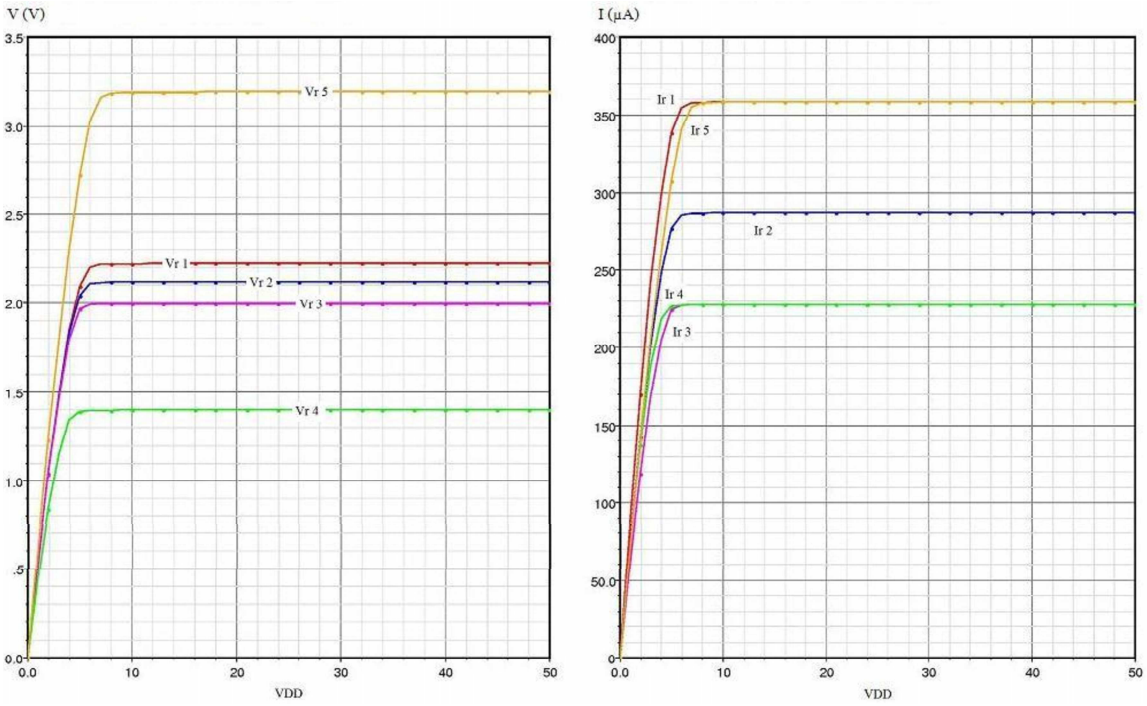

Figure 2.16: Simulation results using corner analysis. Left: the voltage V_r as a function of the supply voltage V_{DD}. Right: the current I_r as a function of V_{DD}

The different curves are the results of an applied worst case analysis. Assuming that worst cases are corners of the parameter range a corner analysis delivers results which may occur very unlikely. That means that the worst case analysis can be very pessimistic

in terms of probability. The advantage of this analysis is the fast simulation time due to the easy model extraction.

The following table shows the parsed worst cases of Fig. 2.16.

Table 2.7: Voltage V_r with varied worst cases

Curve	cmos	resistance	temperature
V_{r1}	typ	typ	typ
V_{r2}	wp	wp	typ
V_{r3}	ws	ws	typ
V_{r4}	wp	ws	typ
V_{r5}	ws	wp	typ

Note: wp: worst power, ws: worst speed

In contrast to worst cases analysis a Monte Carlo analysis allows the investigation of process and device mismatch. The simulation results are more likely to occur in reality. A typical Monte Carlo simulation generates several multivariate random samples of the parameter vector and performs the desired circuit analysis for each sample. The curves of the samples are all bounded by the characteristics of corner simulation shown in Fig. 2.17.

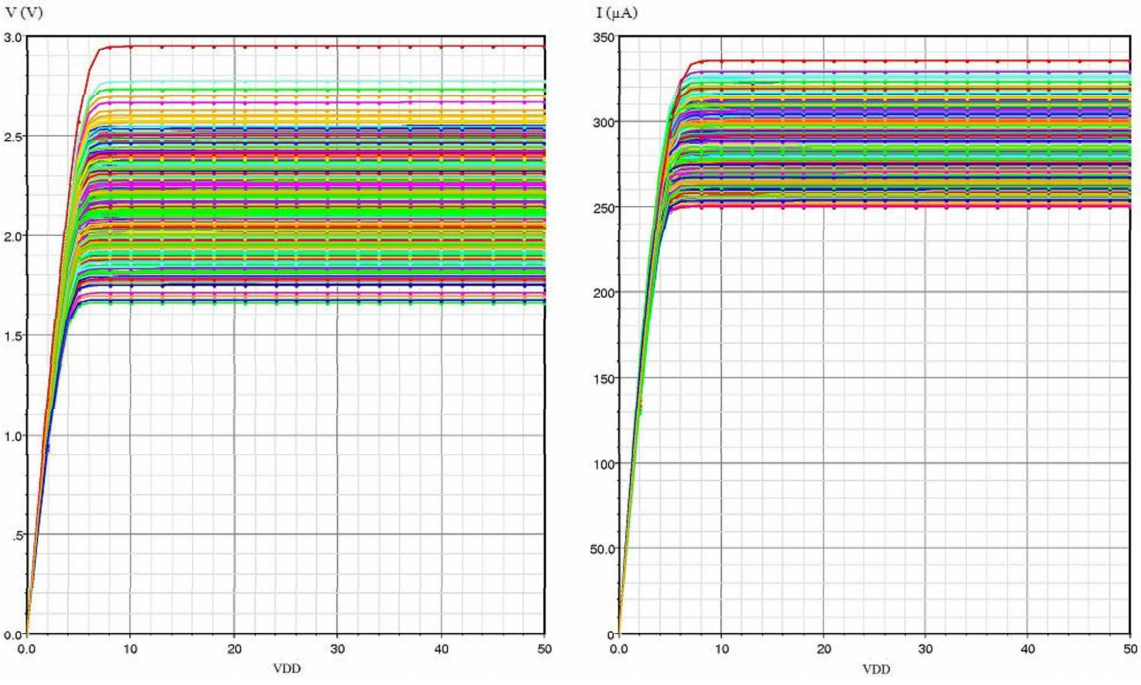

Figure 2.17: Simulation results using Monte Carlo analysis. Left: the voltage V_r as a function of the supply voltage V_{DD}. Right: the current I_r as a function of V_{DD}

As shown in Tab. 2.7 the temperature is always set to a typical value. As claimed in the specifications, the analog switch of the matrix test chip has to be functional between minimum and maximum temperatures of $-40°C$ and $+125°C$. Involving these values in the worst case simulation, unsatisfying results are achieved. The derived values of

the voltage V_r exceed the maximal allowed gate-source voltage of the p-channel MOS transistor. The main problem is that V_r is varying with both, the current and the resistance, so the effects of worst cases redouble. To reduce the temperature dependence of the level shifter two pn-junctions of the base-emitter-diode of the vertical npn-transistor VERTN1 have been added to the circuit, as shown in Fig. 2.18.

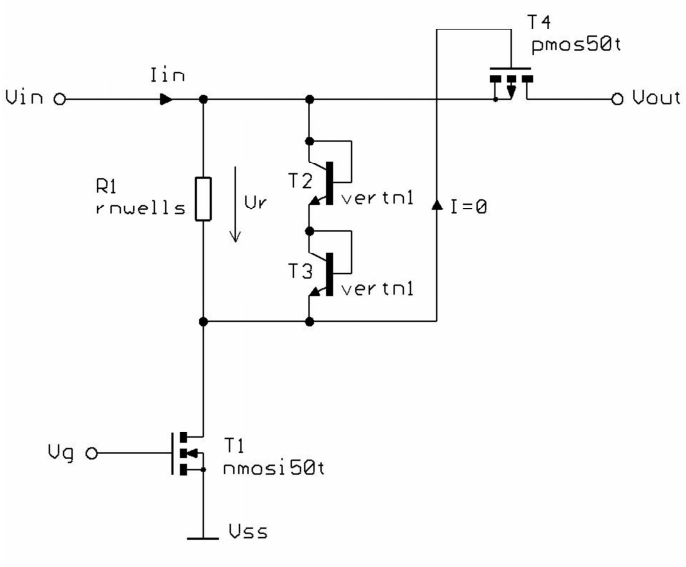

Figure 2.18: Level shifter with 2 vertn1-junctions to reduce temperature dependence

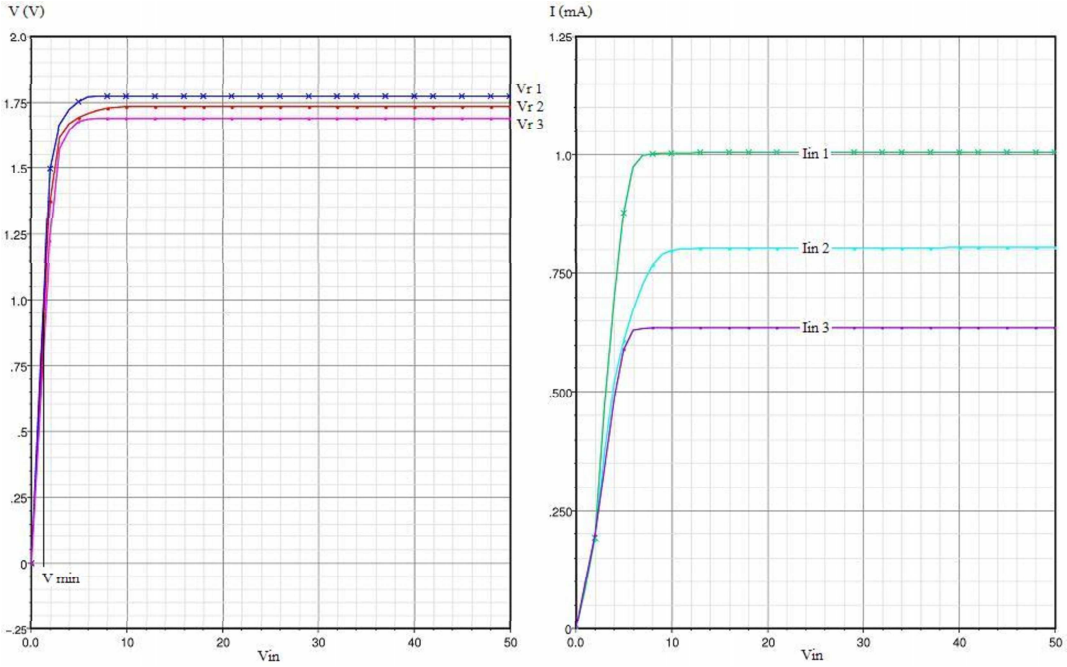

Figure 2.19: Simulation results with corner analysis. Left: the voltage V_r as a function of the supply voltage V_{in}. Right: the current I_{in} as a function of V_{in}

The pn-junctions decrease the dispersion of the voltage V_r $(= V_{GS_{T4}})$ to the tenth part. There is also an improvement in stability. The gate-source voltage now depends only on the temperature coefficient of the pn-junction of the npn transistors $T2$ and $T3$, which is approximately $\Delta V_{BE} = -2mV/K$. The resistor $R1$ guarantees that the potential on the gate of $T4$ is following the input voltage to avoid a breakdown in the OFF state

where $V_g = 0$. Illustrated by the V_r curve of Fig. 2.19 the voltage V_{min} represents the minimum input voltage to ensure that the pMOS-switch is ON. For lower input voltages the transistor is in the off-state. To ensure the on-state for $V_{in} < V_{min}$ the circuit has to be extended.

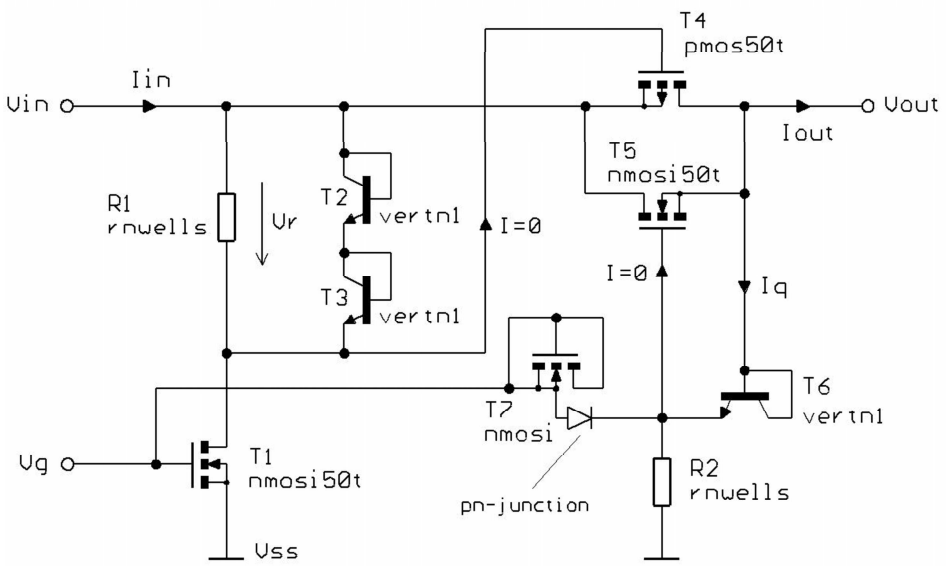

Figure 2.20: Enhanced level shifter with a t-gate

$T4$ and $T5$ now form a typical t-gate. In the ON state, the n-channel device $T5$ should be conductive for the lower input voltage range. Therefore, some additional components are necessary. As shown in Fig. 2.20 a pn-junction of the isolated nMOS transistor $T7$ is used. The connected gate, bulk, source and drain terminals of $T7$ represent the anode of the diode. The isolated n-well of the transistor is the cathode of the pn-junction. If the control voltage V_g of the logic circuit is high, $V_g = 3.3V$, the current through the diode and the resistor $R2$ generates a voltage drop. This potential causes the transistor $T5$ to be conductive independent of $V_{in} < V_{min}$. For high input voltages applied, the p-channel device $T4$ will be conductive so that V_{out} follows V_{in}. If $V_{out} - V_{pn_{T6}} > V_g - V_{pn_{T7}}$ the potential on the gate of $T5$ follows the output voltage. Here the npn transistor $T6$ avoids a gate-source breakdown of the device $T5$.

Assumed that the output terminal of the analog switch is connected with the gate of a test device in MOS technology, the output current

$$I_{out} = I_G = 0 \tag{2.16}$$

The current I_q is used to shift the gate-voltage of the transistor $T5$ together with V_{out} in the upper operating range. This current flows through the t-gate and generates a voltage drop $V_{R_{ON}}$ at the ON resistance which reduces the accuracy.

$$V_{out} = V_{in} - V_{R_{ON}} \;,\; V_{R_{ON}} = I_q \left(R_{ON_{T4}} \| R_{ON_{T5}}\right) \tag{2.17}$$

$$Ideal: \; V_{R_{ON}} = 0 \rightarrow V_{out} = V_{in}$$

$$Real: \; V_{R_{ON}} > 0 \rightarrow V_{out} < V_{in}$$

The voltage drop $V_{R_{ON}}$ could be decreased using a larger W/L ratio, but this would cause an enlargement of the space requirements. Now, the opportunity arises to replace the resistor $R2$ by an isolated high voltage nMOS device (NMOSI50T), see $T8$ in Fig. 2.21.

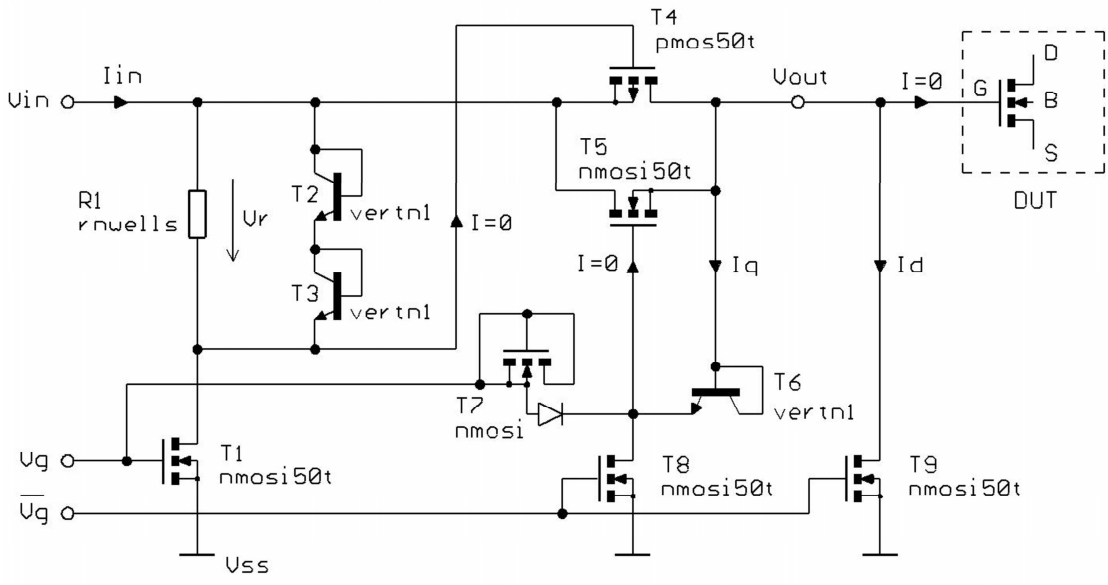

Figure 2.21: Final used analog switch with t-gate and level shifters

The use of parasitic devices of the MOS transistor which are normally undesirably is the specialty of this circuit. For the design the parasitic high voltage p-well to deep n-tub diode is used. This diode is implemented in the NMOSI50T model for simulation of reverse leakage currents and junction capacitances. Here is a brief description of the functioning. If V_g is high and $V_{out} - V_{pn_{T6}} > V_g - V_{pn_{T7}}$ the basis-emitter-diode of $T6$ starts to conduct. The current I_q depends on the voltage $u(t)$ (here $V_{DS_{T8}}$) and the parasitic capacitance C_j

$$i_q = C_j(u(t)) \frac{du(t)}{dt} + u(t) \frac{dC_j(u(t))}{dt} \tag{2.18}$$

I_q recharges the capacitance C_j as far as the voltage V_{in} is varied. If $V_{in} = const$ the current decreases exponential to 0 involving a minimization of the voltage drop $V_{R_{ON}}$. Additionally, the transistor $T8$ ensures that the potential on the gate of the nMOS device $T5$ is zero in the OFF state. To avoid a recharge of parasitic capacitances on the output terminal in the OFF state $T9$ shorts the voltage on the gate of the DUT to the p-substrate-potential.

The following figures (Fig. 2.22 to Fig. 2.30) illustrate the behaviour of node voltages and device currents depending on the input voltage. They show the calculated values of

the simulation and the measured values in the OFF and ON state. The files with the extension *.dat* represent the measurement data files, the *.new* files refer to the computed results (see legend). Fig. 2.22 and Fig. 2.23 show the behaviour of the gate voltage of the p-channel MOS transistor $T4$. In the OFF state the current through the resistor $R1$ is zero. Just as the voltage drop V_r, so equal potential is on the gate and on the input terminal and $T4$ is switched off. In the ON state the gate voltage is two pn-junction-voltages below the input voltage, assuming $T1$ is in the saturation region.

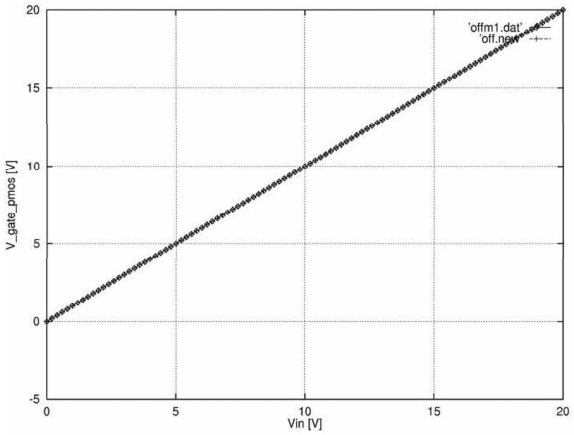

Figure 2.22: V_{Gate} of T4 as a function of V_{in}, OFF state, $\diamond$ measurement data, + simulation data

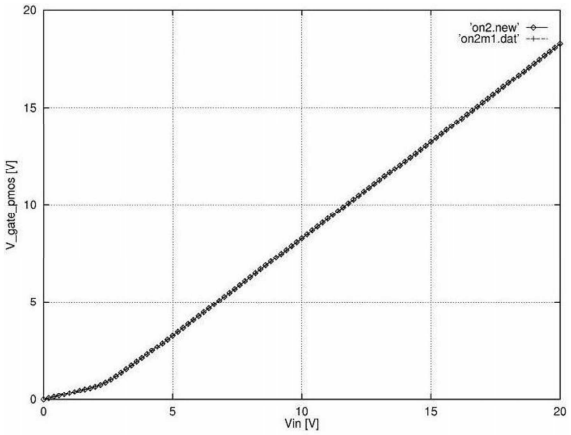

Figure 2.23: V_{Gate} of T4 as a function of V_{in}, ON state, $\diamond$ measurement data, + simulation data

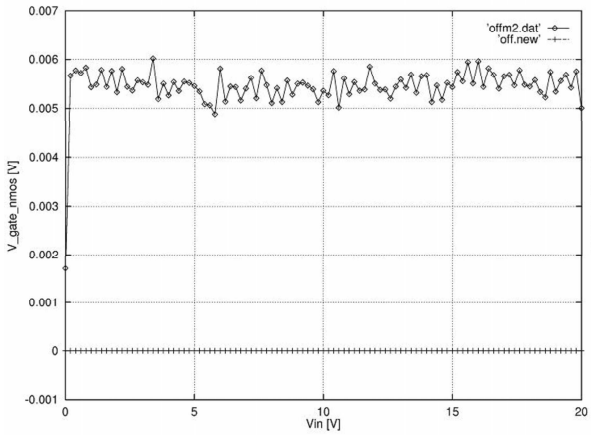

Figure 2.24: V_{Gate} of T5 as a function of V_{in}, OFF state, $\diamond$ measurement data, + simulation data

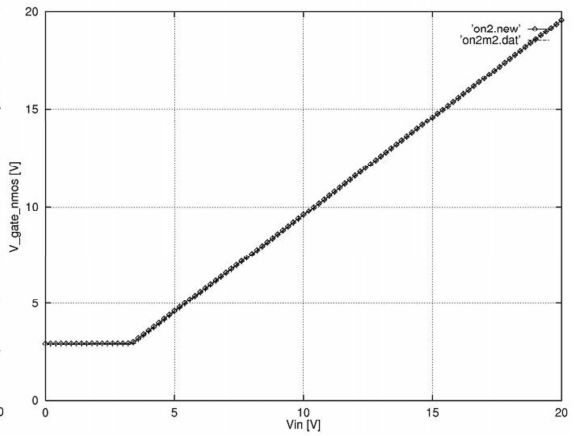

Figure 2.25: V_{Gate} of T5 as a function of V_{in}, ON state, $\diamond$ measurement data, + simulation data

As illustrated in Fig. 2.24 the gate voltage of the nMOS device $T5$ is nearly zero when Vg is low ($T8$ is on). The measured values are higher than the simulated data primarily caused by the short integration time of the PA. In the ON state the curves in Fig. 2.25 can be divided in two sections. For input voltages below the inflexion point ($V_{in} \approx 3.5V$) the gate voltage is approximately $V_g - V_{pn_{T7}}$. Beyond this input voltage the potential on the gate is following the output voltage (caused by the pn-junction of $T6$).

The next figures (2.26 and 2.27) show the behaviour of the input current depending on the input voltage. In Fig. 2.26 the calculated values give a resistance curve caused by the resistance R_{OFF} of the implemented MOSFET model (mainly of $T1$). The measured data points approximately have the same magnitude. If the analog switch is on the curve of the current I_{in} shows a linear behaviour for small input voltages applied and gets saturated if V_{in} is increased. Beyond the linear region the current depends on the characteristics of the shunt circuit of $R1$ and $T2$-$T3$, followed by the saturation effect of the transistor $T1$. For input voltages beyond $V_{in} \approx 3.5V$ the pn-junction of $T6$ becomes conductive and the inaccuracy of the NMOSI50T model causes the difference of the computed and measured curve.

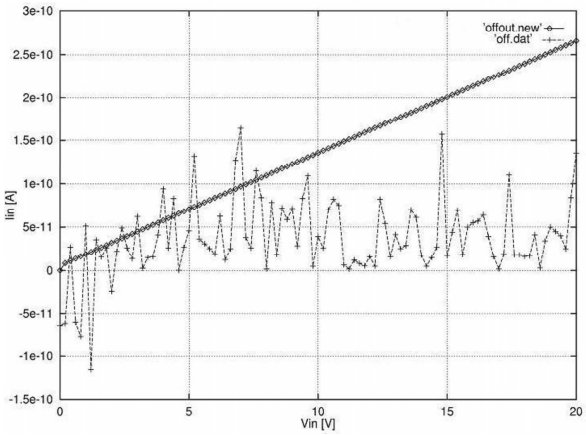

Figure 2.26: I_{in} as a function of V_{in}, OFF state , + measurement data, ◇ simulation data

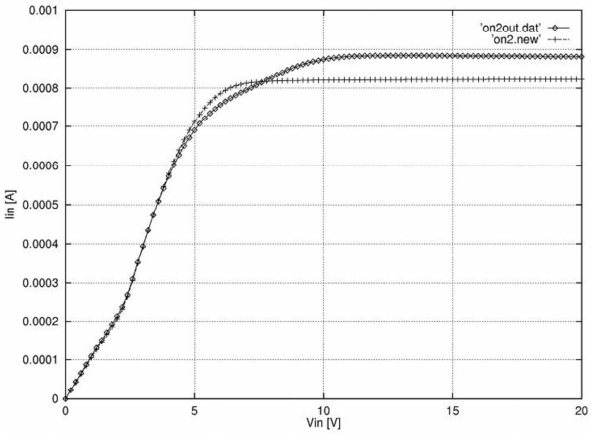

Figure 2.27: I_{in} as a function of V_{in}, ON state , ◇ measurement data, + simulation data

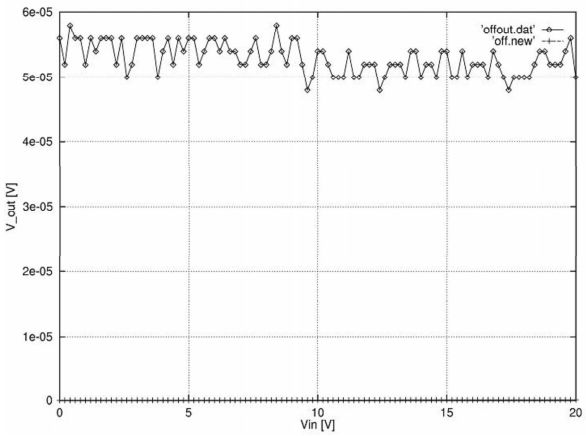

Figure 2.28: V_{out} as a function of V_{in}, OFF state, ◇ measurement data, + simulation data

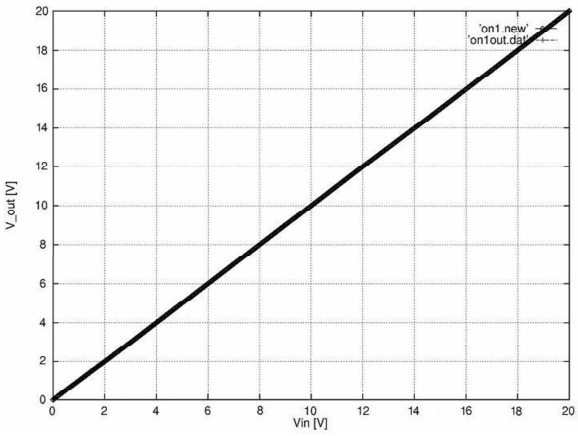

Figure 2.29: V_{out} as a function of V_{in}, ON state, ◇ measurement data, + simulation data

Fig. 2.28 and 2.29 simply illustrate the voltage of the output terminal V_{out} in the OFF and ON state. If the analog switch is off, the measured data points are characteristic for inaccuracies of source unit and measurement unit. However, in the ON state V_{out} follows the input voltage exactly.

To distinguish the difference of the two voltage curves a separate plot was performed. In Fig. 2.30 the voltage drop on the ON resistance of the t-gate is shown. As illustrated the simulation data differs slightly from the measured voltage curve depending on the measurement inaccuracy in the high voltage range of the source monitor unit (SMU) of the PA.

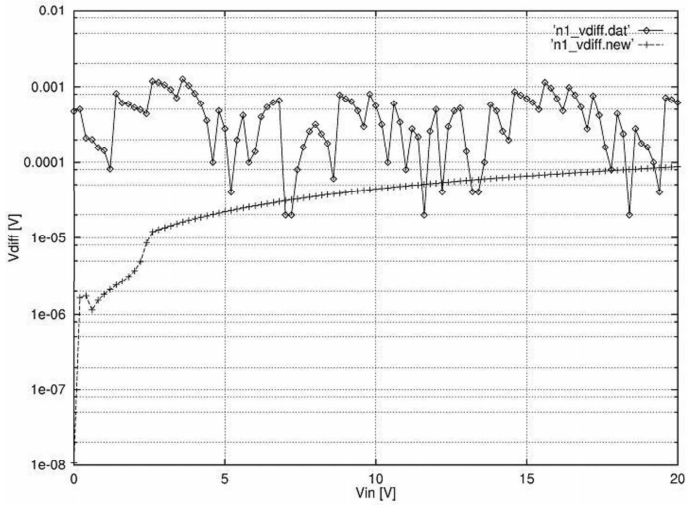

Figure 2.30: V_{diff} as a function of V_{in}, ON state $\diamond$ measurement data, + simulation data

Additionally to the above plots the following figures will show the behaviour of the circuit in Fig. 2.21 in detail. Therefore a transient analysis $(0 \ldots 200ms)$ was made in the OFF and ON state. The input voltage $V_{in} = 20V$ was applied from $t = 10 \ldots 110ms$.

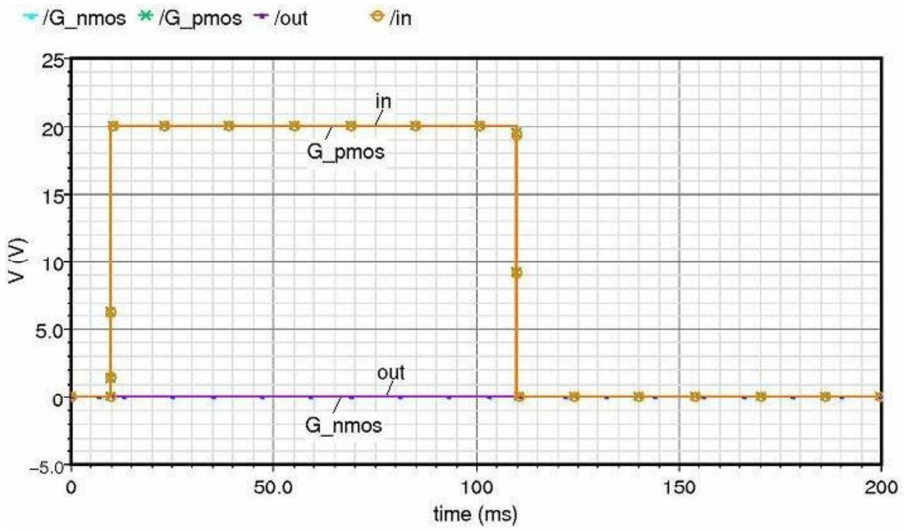

Figure 2.31: *G_pmos:* gate-potential of transistor T4, *G_nmos:* gate-potential of transistor T5, *in*: input voltage, *out:* output voltage, OFF state

As shown in Fig. 2.31 in the OFF state the potential on the gate of $T4$ follows the input voltage. The output voltage and the potential on the gate of $T5$ are zero. That implies that voltage drop on the t-gate is equal to the pulse of the input voltage of the analog

switch (see Fig. 2.32).

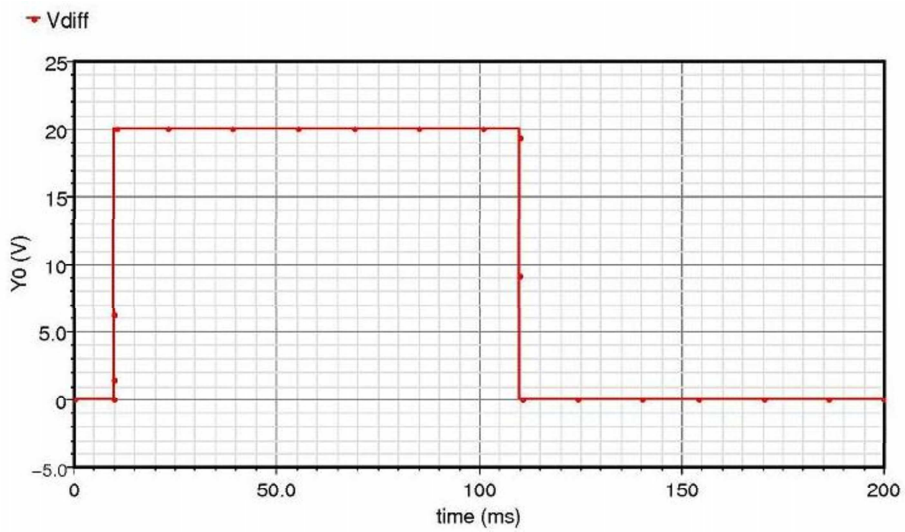

Figure 2.32: *Vdiff*: voltage between input and output terminal, OFF state

As illustrated in Fig. 2.33, the potentials on the gates of the transistors $T4$ and $T5$ behave as anticipated in the ON state. Additionally, the output voltage is equal to the pulsed input voltage.

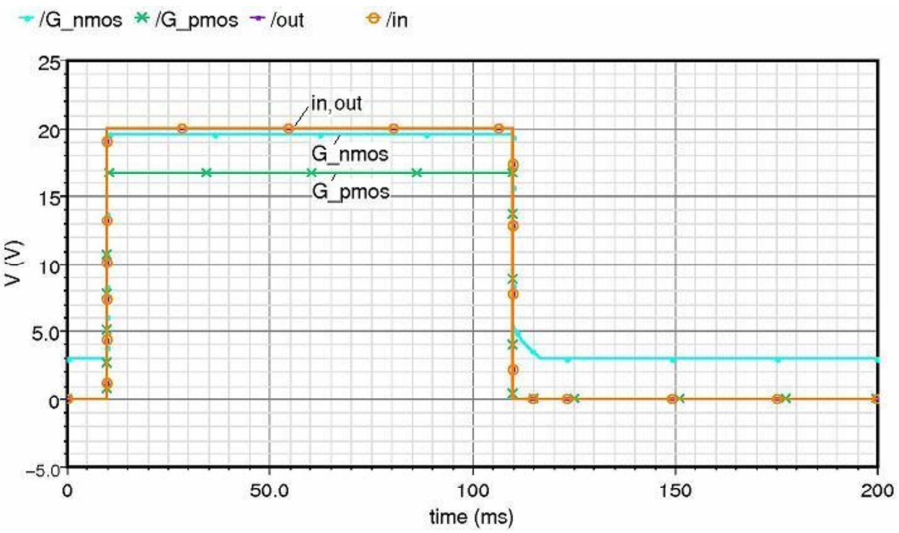

Figure 2.33: *G_pmos:* gate-potential of transistor T4, *G_nmos:* gate-potential of transistor T5, *in*: input voltage, *out:* output voltage, ON state

The offset voltage of the analog switch depends on the current through the t-gate and the resistance R_{ON} of the t-gate. For the simulation of the analog switch simply a load resistor with a resistance of $1G\Omega$ was added to the circuit. Fig. 2.34 shows the time dependency of the offset voltage when the input voltage is pulsed. As illustrated, there are voltage peaks at the start-up and the turn off of the input voltage. These voltage peaks are typical for a low-pass filter consisting of R_{ON} and the parasitic capacitances of $T8$.

The value of the offset voltage of the t-gate (assumed that $R_{ON} \approx 25k\Omega$) is approximately given by

$$V_{diff} = I_{t-gate}\, R_{ON} = \frac{V_{in}}{R_{ON} + R_{LOAD}}\, R_{ON} = \frac{20V}{25k\Omega + 1G\Omega}\, 25k\Omega \approx 50\mu V \quad (2.19)$$

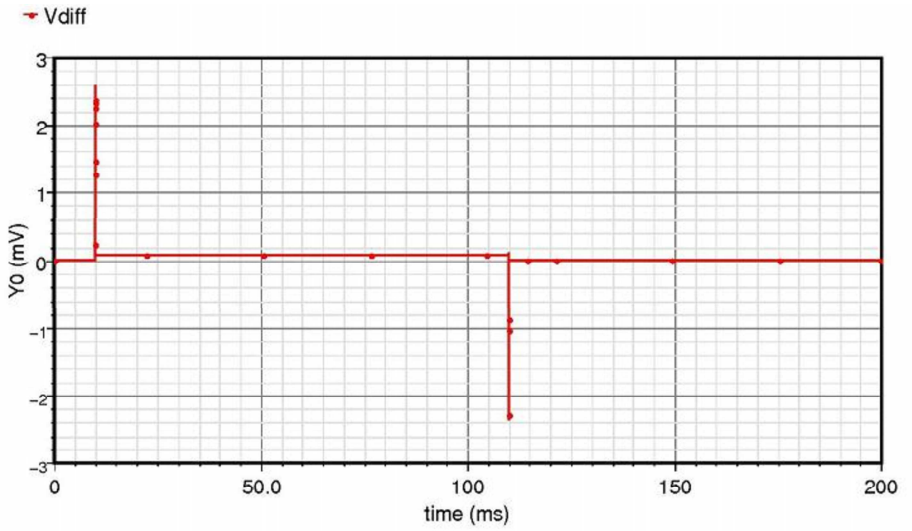

Figure 2.34: *Vdiff*: voltage between input and output terminal, ON state

Subsequently a transient analysis of the whole test matrix circuit shown in Fig. 2.39 was done. To ensure the function of the master design also a corner analysis was implemented. Therefore, a combination of the most critical corners of the models were performed, shown in Tab. 2.8 ($T_{min} = -40°C$, $T_{max} = 125°C$).

Table 2.8: Corner overview of Fig. 2.35 ... 2.38

CORNER	CMOS53	RES	TEMP
Corner1	cmostm	restm	typ
Corner2	cmoswp	reswp	min
Corner3	cmosws	resws	min
Corner4	cmoswp	resws	min
Corner5	cmosws	reswp	min
Corner2b	cmoswp	reswp	max
Corner3b	cmosws	resws	max
Corner4b	cmoswp	resws	max
Corner5b	cmosws	reswp	max

For the simulation of the whole test circuit following settings and values were used:

Switch ON : $1 \ldots 4ms$

Simulation time : $0 \ldots 5ms$

V_{in} *const* : $15V$

The next plots show the behaviour of the circuit in all cases of corners summarized in Tab. 2.8. In Fig. 2.35 the time behaviour of the input current is shown. Its values are negative caused by an outgoing current of voltage source V_{in} in the simulation.

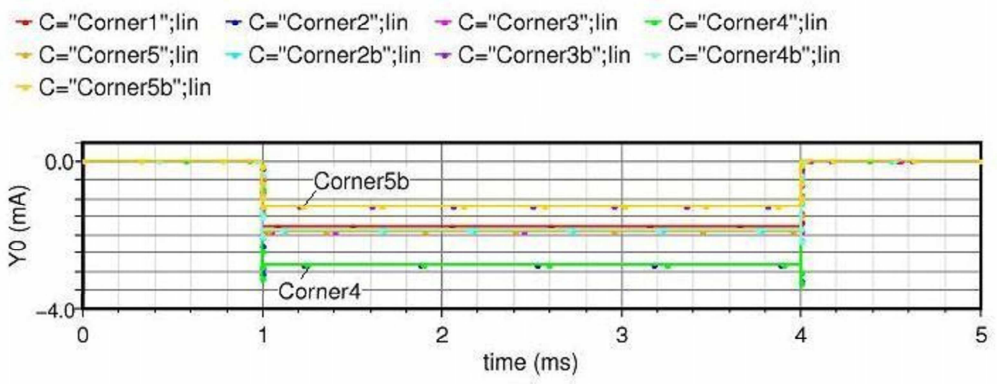

Figure 2.35: Worst cases of the input current I_{in}, transient analysis

The potentials on the gate of the t-gate-transistors $T5$ ($Gnmos$) and $T4$ ($Gpmos$) are shown in Fig. 2.36 and 2.37. The most critical corners are $Corner4$ and $Corner5b$ of Tab. 2.8. $Corner4$ defines the lower bound, $Corner5b$ defines the upper bound of the range.

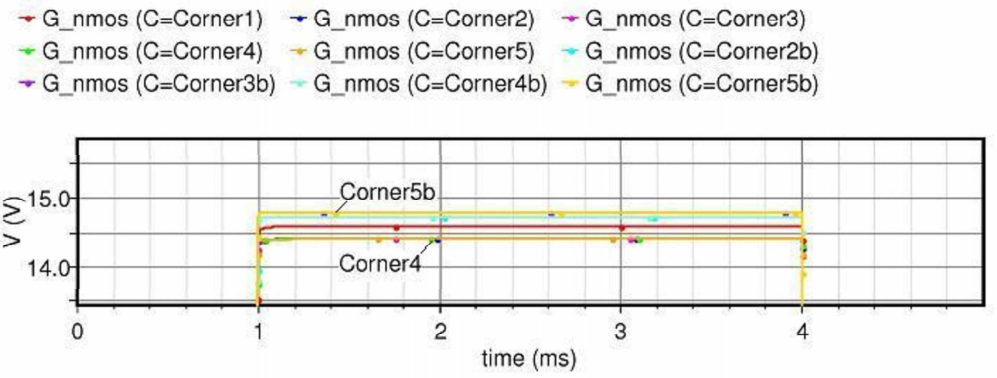

Figure 2.36: Worst cases of the gate voltage of $T5$ ($Gnmos$), transient analysis

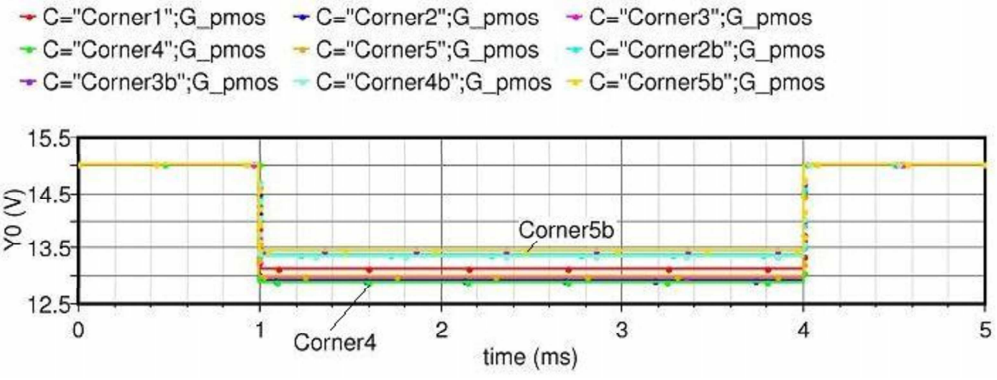

Figure 2.37: Worst cases of the gate voltage of $T4$ ($Gpmos$), transient analysis

The voltage drop $Vdiff$ on the t-gate of the analog switch is illustrated in Fig. 2.38. As shown the most critical corners of the offset voltage are different to the ones discussed before. The corners $Corner2b$ and $Corner4b$ have the same CMOS53 corners ($worst\ power$) and the same temperature corner ($Tmax$). This indicates that a maximum of the offset voltage is reached by $I_{DS}max$ and $Tmax$. The worst case power leads to a maximum of the channel-current I_{DS} and the voltage drop, respectively.

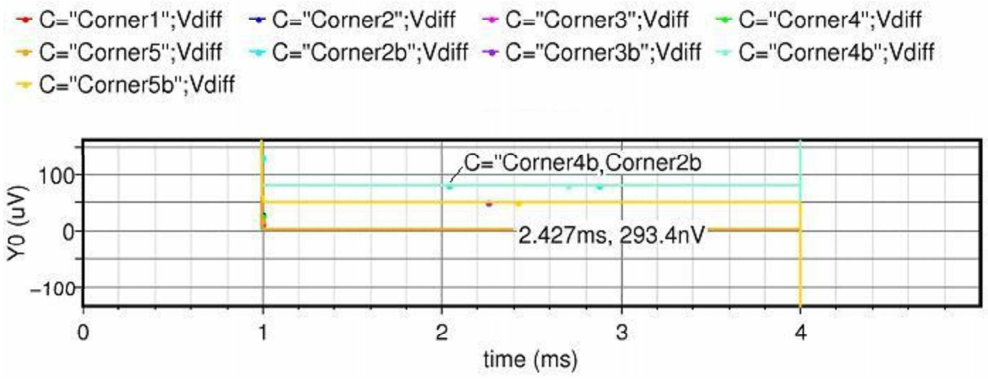

Figure 2.38: Worst cases of the offset voltage V_{diff} of the analog switch, transient analysis

Fig. 2.39 shows the schematic of the whole test circuit design including the DUTs. The first block of the circuit (from left to right) is the digital part consisting of one 8-bit shift register. The digital signal controls the 8 analog switches represented in one block named *logic_gate*. Therefore, all connections are one bus-wire (thick line). Below there is another block which is not connected with the remaining parts of the circuit to facilitate measurements. On the right hand side there are two columns with devices under test for characterization.

The layout of the schematic is illustrated in Fig. 2.40. The test macro has 16 contact pads (see Tab. 2.10) for a special probe card and 5 pads (M1..M5) to measure significant voltages inside the analog switch circuit (see Tab. 2.9).

Table 2.9: Assignment of the measuring pads and the signals (Fig. 2.21)

Contact pad	M1	M2	M3	M4	M5
Signal	V_g	$\overline{V_g}$	$V_{Gate_{T4}}$	$V_{Gate_{T5}}$	V_{out}

The signal pads 1..5 are reserved for the digital signals of the logic block. Since the first test macro has only one column of DUTs, pad 4 and 5 can be applied for a second drain force-sense terminal facilitating a second column with devices for testing. Pad 6 connects the ground potential of the test chip to the ground of the probe card (force/sense). The supply voltage of the digital block is connected to pad 7, the power supply of the pMOS-switch, V53 (see Tab. 2.10) is connected to pad 8. The following pads (9..16) are reserved for the force and sense input signals of the measurement terminals.

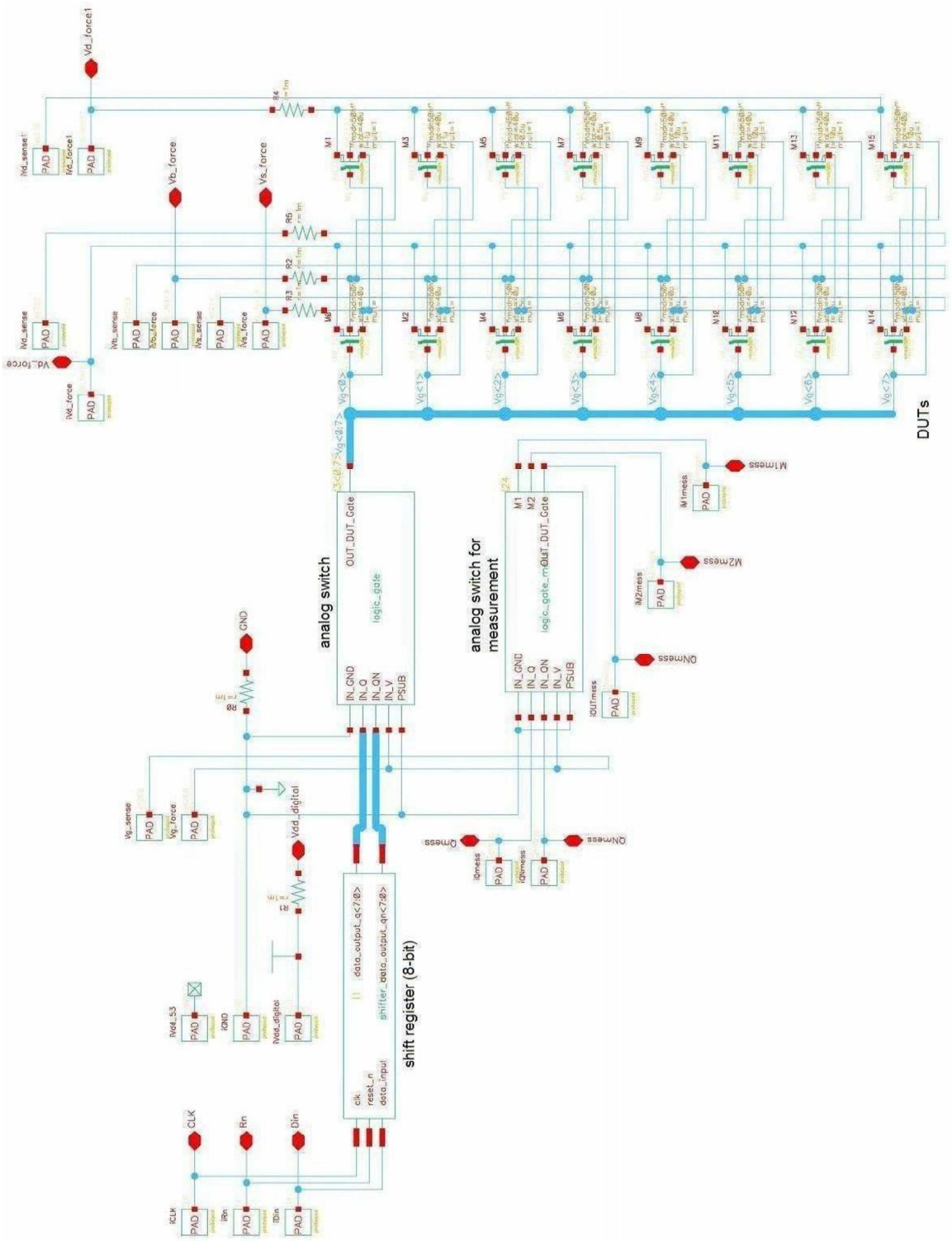

Figure 2.39: Schematic of the analog circuit design

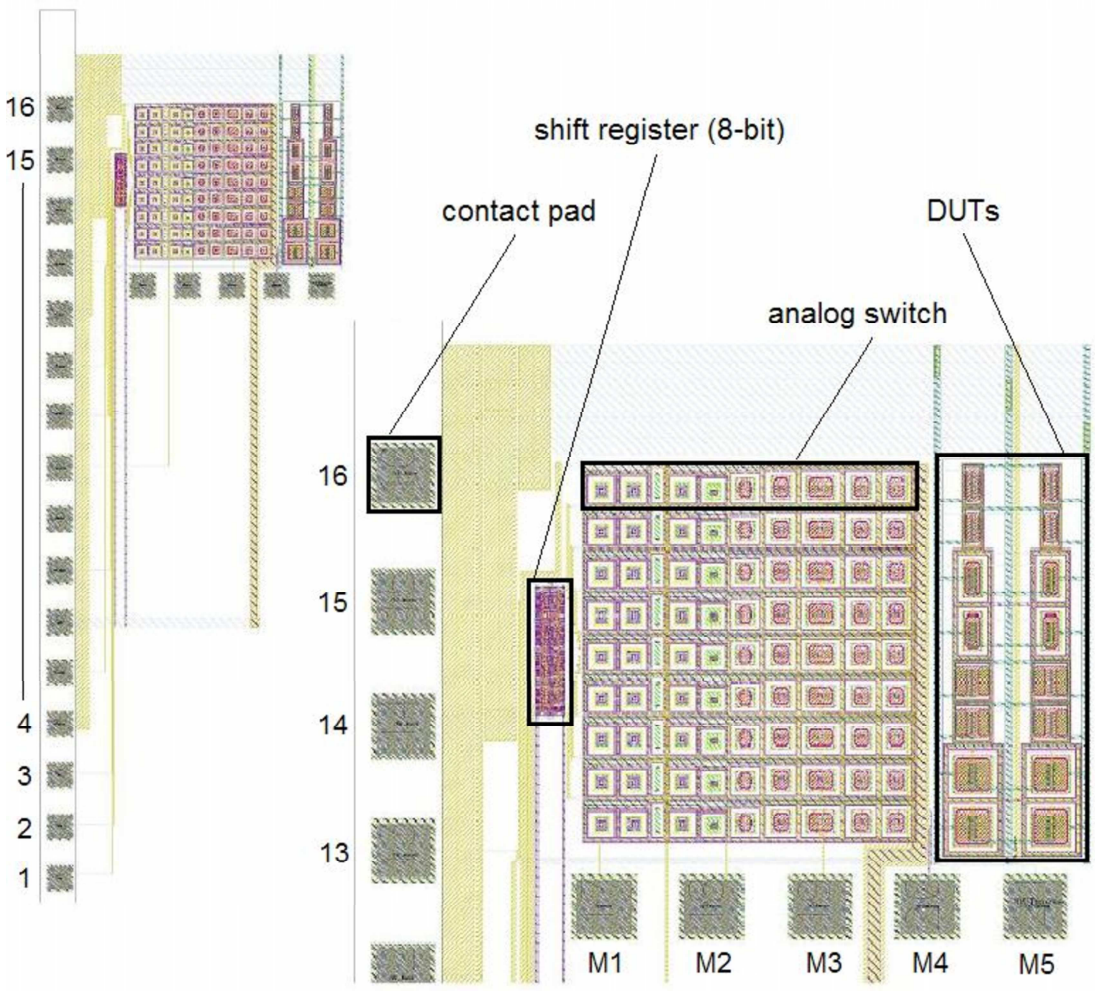

Figure 2.40: Layout of the analog circuit design

Table 2.10: Assignment of the contact pads and the signals

Contact pad no	Signal
1	Rn ..... Reset of the logic block
2	Clk 0 .. Clock input for index i of the test matrix
3	Din 0 .. Data input for index i if the test matrix
4	Clk 1 .. (V_{D2} force) Clock input for index j (2nd Drain force)
5	Din 1 .. (V_{D2} sense) Clock input for index j (2nd Drain sense)
6	GND .... Ground potential (p-sub)
7	Vdd .... Power supply for the digital block (3.3/5V)
8	V53 .... Power supply for the pMOS - switch
9	Vgs .... Sense input of the gate voltage (DUT)
10	Vgf .... Force input of the gate voltage (DUT)
11	Vbs .... Sense input of the bulk voltage (DUT)
12	Vbf .... Force input of the bulk voltage (DUT)
13	Vss .... Sense input of the source voltage (DUT)
14	Vsf .... Force input of the source voltage (DUT)
15	Vds .... Sense input of the drain voltage (DUT)
16	Vdf .... Force input of the drain voltage (DUT)

As illustrated above the gate voltage of the DUT is nearly zero if using the analog switch for nMOS test devices in the OFF state. Using p-channel transistors for testing would cause a problem. To measure these devices negative drain voltages would be needed but potentials below the substrate-voltage (ground, V_{SS}) are not permitted. So the source of the device under test has to be biased to higher potentials which is in our case $V_S = 50V$. Therefore, the gate of the test device has to be set to $V_G = 50V$ if the switch is off. For this reason it is necessary to modify the previously discussed 'analog switch for nMOS transistors' design.

2.7 Design for p-channel MOS transistors

As mentioned above the voltages needed for measuring a p-channel MOS transistor differ from the voltages provided by nMOS-switch. The voltage range on the gate of high voltage nMOS devices is $V_{GS} = 0 \ldots 20V$ maximum at $V_S = 0V$, $V_D = 0 \ldots 50V$. The gate potentials of high voltage p-channel MOS transistors are $V_G = 50 \ldots 30V$ maximum at $V_S = 50V$, $V_D = 50 \ldots 0V$. The following schematics and plots deal with necessary modifications and the redesign of the analog switch discussed before (see Fig. 2.21).

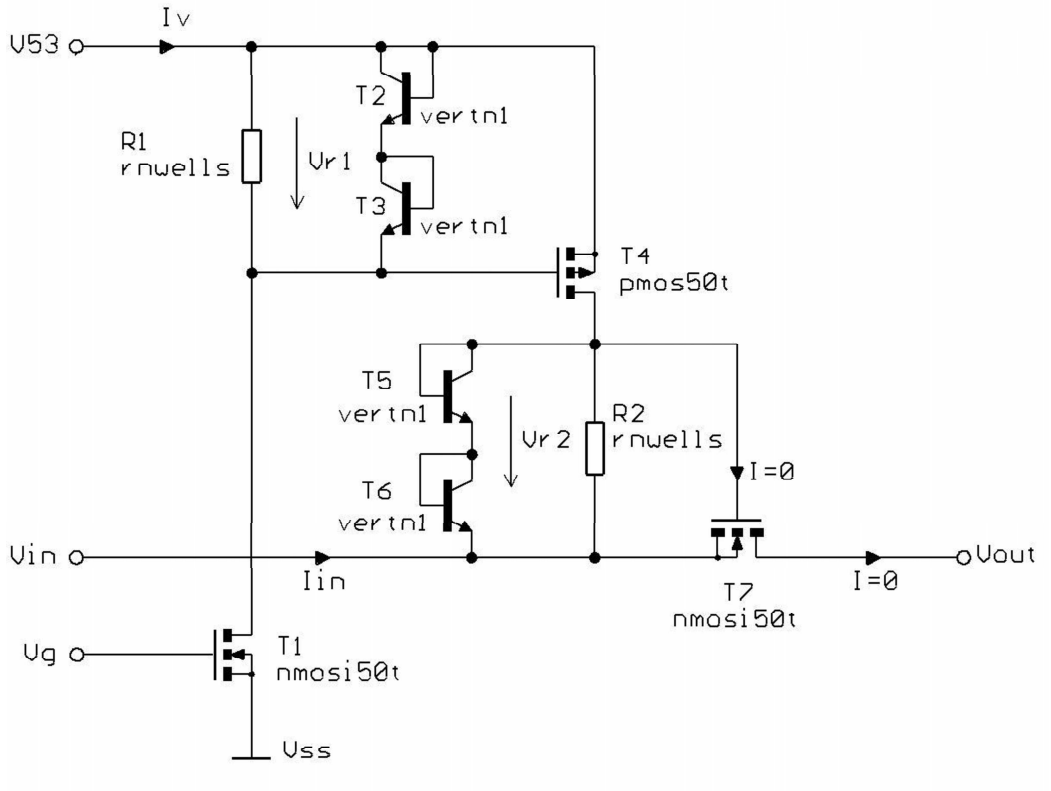

Figure 2.41: Analog switch for p-channel-devices, first design

As shown in Fig. 2.41 in this design there is an equivalent current sink consisting of transistor $T1$ and the resistor $R1$. In the ON state, V_g is high, the voltage drop V_{r1} $(= -V_{GS_{T4}})$ ensures that the transistor $T4$ is on. V_{r1} depends on the diffusion voltages of the pn-junctions of $T2$ and $T3$, which avoid a gate-source-breakdown of $T4$ for all kinds of worst cases. Now, the specialty is the level shifter element in the input circuit

consisting of the devices $R2$, $T5$ and $T6$. Applying an input voltage, a current from the power supply $V53$ flows through the shunt circuit mentioned before (I_G of $T7$ is zero). The npn transistors $T5$ and $T6$ now generate a constant voltage drop which can be shifted with the voltage V_{in}. It is mainly influenced by the chip temperature. Thus it appears that the potential on the gate of $T7$ is higher than the input voltage ($V_{r2} > V_{th}$). So $T7$ is on and the output voltage follows the input voltage. The voltage drop of the level shifter element in the ON state is illustrated in Fig. 2.42 (worst case analysis) and Fig. 2.43 (Monte Carlo analysis).

In the OFF state (V_g is low) the voltage drop V_{r1} is zero. That implies that the gate-source-voltage of the transistor $T4$ is below its threshold voltage, so $T4$ is off. This indicates that the input current $I_{in} = 0$ and also $V_{r2} = V_{GS_{T7}} = 0$, meaning $T7$ is off.

The potential on the gate of the transistor $T7$ is given by

$$V_{Gate_{T7}} = V_{in} + V_{r2} \rightarrow V_{out} = V_{in} \tag{2.20}$$

in the ON state and

$$V_{Gate_{T7}} = V_{in} \rightarrow V_{out} = 0 \tag{2.21}$$

in the OFF state.

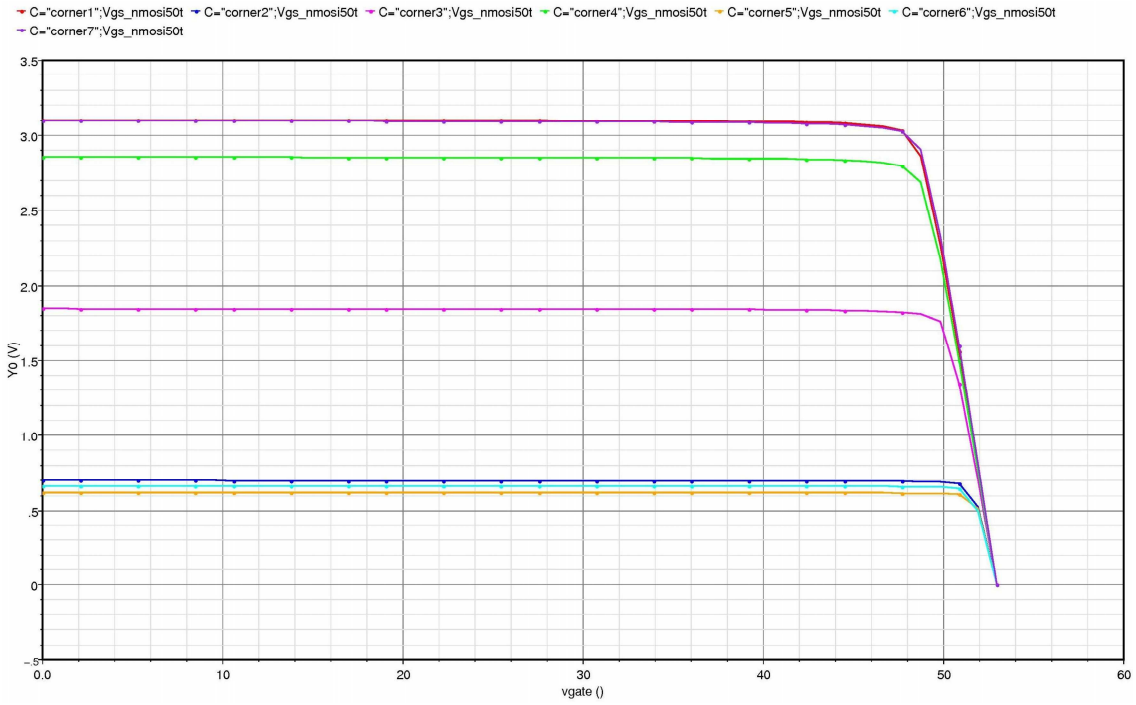

Figure 2.42: V_{r2} as a function of the input voltage V_{in}

As illustrated in Eq. (2.21) the output voltage connected on the gate of the test device

is zero when the switch is off. This would cause a gate-source-breakdown ($V_{G_{DUT}} = 0V,\ V_{S_{DUT}} = 50V$) of the p-channel MOS transistor which should be characterized. To avoid this problem some modifications were performed.

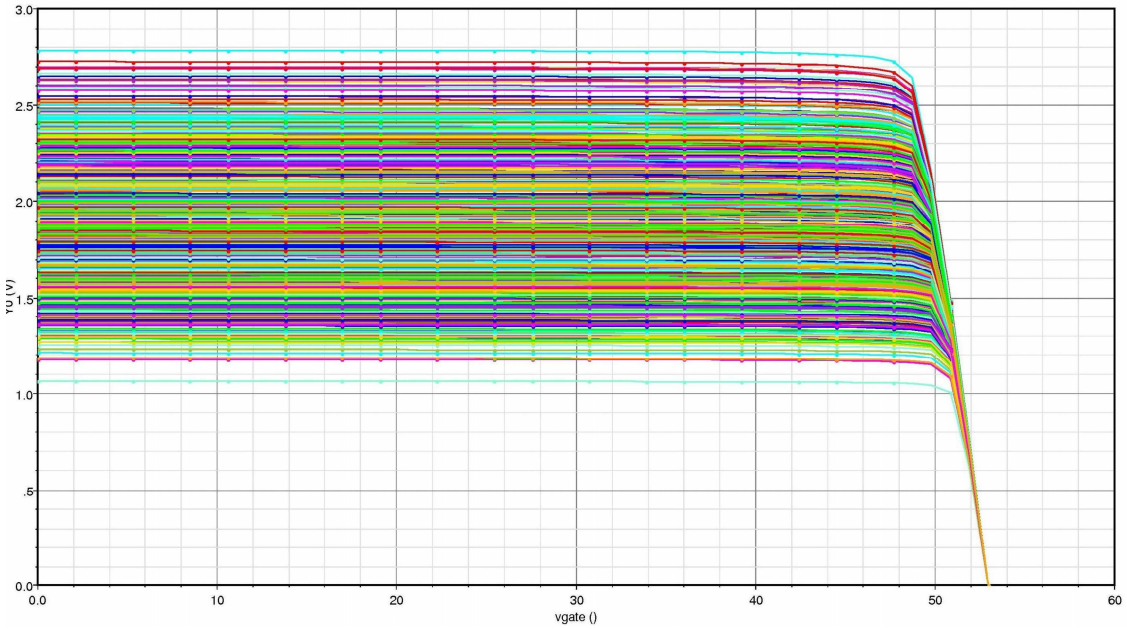

Figure 2.43: V_{r2} as a function of the input voltage V_{in}

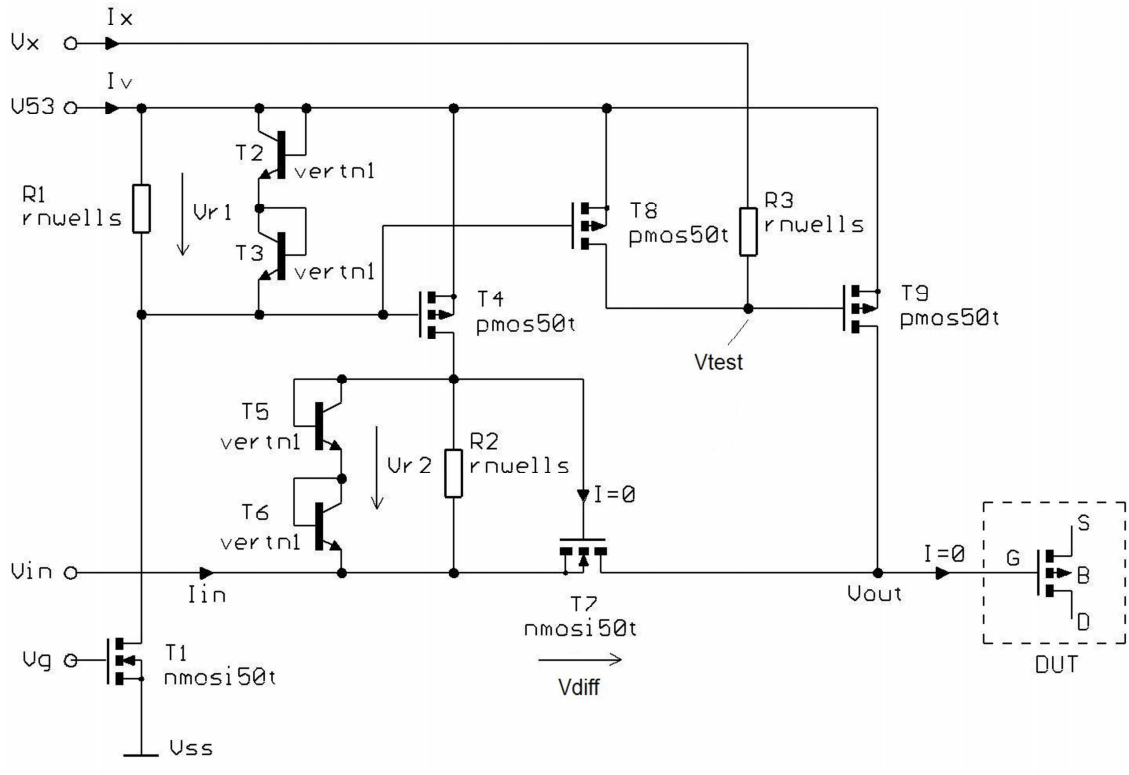

Figure 2.44: Finally used analog switch for p-channel-devices

As shown in Fig. 2.44 the resistor $R3$ and the transistors $T8$ and $T9$ were added. Their

function was described with the Fig. 2.45.

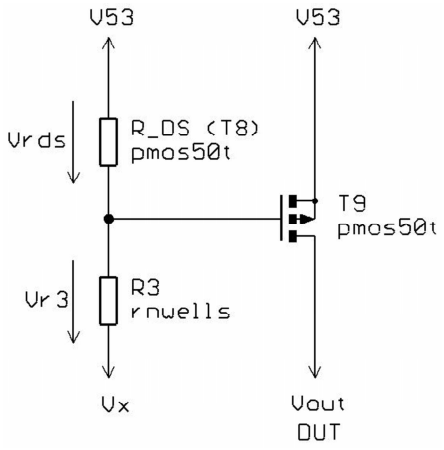

Figure 2.45: Function of $R3$, $T8$ and $T9$ of the used design

The chosen W/L ratio of the resistor $R3$ is 4/40 giving a resistance value of

$$R_3 \approx \frac{L}{W_{eff}} R_{field} = \frac{40}{4.3} 1.33k\Omega/\square = 12.372k\Omega \tag{2.22}$$

to guarantee the following potentials of important circuit nodes:

In the ON state ($T8$ on): $R_{DS} + R_{i_{V53}} < R_3 + R_{i_{Vx}}$

$$V_{RDS} < V_{R3} \Rightarrow V_{GS_{T9}} < V_{th} \Rightarrow \underline{V_{out} = V_{in}} \tag{2.23}$$

In the OFF state ($T8$ off): $R_{DS} + R_{i_{V53}} >> R_3 + R_{i_{Vx}}$

$$V_{RDS} >> V_{R3} \Rightarrow V_{GS_{T9}} > V_{th} \Rightarrow \underline{V_{out} = V53} \tag{2.24}$$

As shown in Eq. (2.23) and (2.24) the output voltage is either the input voltage V_{in} (ON) or the voltage $V53$ (OFF). This new design ensures that the gate-source-voltage does not exceed the breakdown-voltage of $T9$. $R_{i_{V53}}$ and $R_{i_{Vx}}$ are the internal resistances of the voltage sources V53 (outside the chip) and Vx (on the chip). The external resistance $R_{i_{V53}} \approx 0$ and the internal resistance $R_{i_{Vx}}$ is given by

$$R_x \approx \frac{L}{W_{eff}} R_{field} = \frac{165}{4.3} 1.33k\Omega/\square = 51.035k\Omega \tag{2.25}$$

The generation of the voltage V_x is applied on the chip with the circuit in Fig. 2.46. As shown V_x is permanently two diffusion-voltages (pn-junctions of $Tx1$ and $Tx2$) lower

than the forced voltage $V53$. A high resistance value was chosen for R_x to avoid a large supply current I and to ensure the proper potentials in the ON and OFF state.

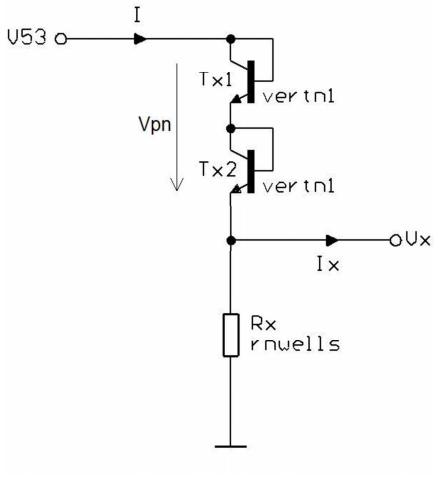

Figure 2.46: Circuit to generate the voltage Vx used by the switch

The following plots illustrate the simulation results of the pMOS-switch-design in Fig. 2.55. Therefore, a transient analysis with additional corner analysis (see Tab. 2.11) was performed. For the simulation of the test circuit the following settings and values were used:

Switch ON : $1 \ldots 6ms$

Simulation time : $0 \ldots 10ms$

V_{in} *const* : $50V$

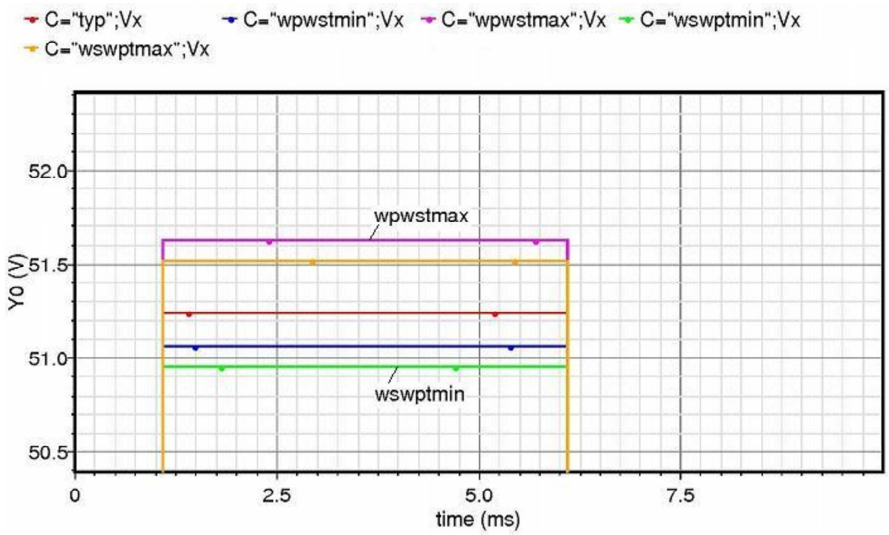

Figure 2.47: Worst cases of the self-generated voltage V_x, transient analysis

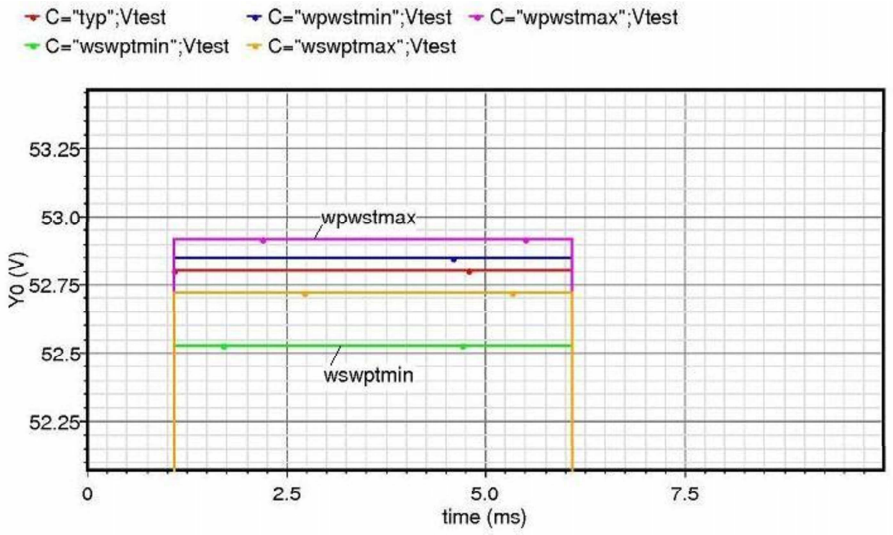

Figure 2.48: Worst cases of the voltage V_{test}, transient analysis

Table 2.11: Corner overview of Fig. 2.47 ... 2.49

CORNER	CMOS53	RES	TEMP
typ	cmostm	restm	typ
wpwstmin	cmoswp	resws	min
wpwstmax	cmoswp	resws	max
wswptmin	cmosws	reswp	min
wswptmax	cmosws	reswp	max

Fig. 2.47 shows the corners of the voltage V_x which ensures that the test device is switched to the voltage $V53$ via the transistor $T9$ in the OFF state. In the ON state the behaviour of the voltage V_{test} on the gate of the transistor $T9$ in the used circuit is very important. V_{test} had to be large enough to ensure that $T9$ is off in the ON state, shown in Fig. 2.48.

The lower bound ($wpwstmax$) and the upper bound ($wswptmin$) define the worst cases of the voltages V_x and V_{test}. This is caused by the low and high resistance value of the resistor $R1$, described by

$$worst-speed \rightarrow R_{max} \rightarrow I_{min} \rightarrow min\ V_{pn} \rightarrow max\ V_x\ (V_{test})$$

$$worst-power \rightarrow R_{min} \rightarrow I_{max} \rightarrow max\ V_{pn} \rightarrow min\ V_x\ (V_{test})$$

using the notations given in Fig. 2.46.

The corners of the offset voltage of the analog switch are shown in Fig. 2.49. The voltage drop mainly depends on the load resistor of the test circuit. The following figures illustrate the measured data compared with the computed data of the simulation ($T = 25°C$).

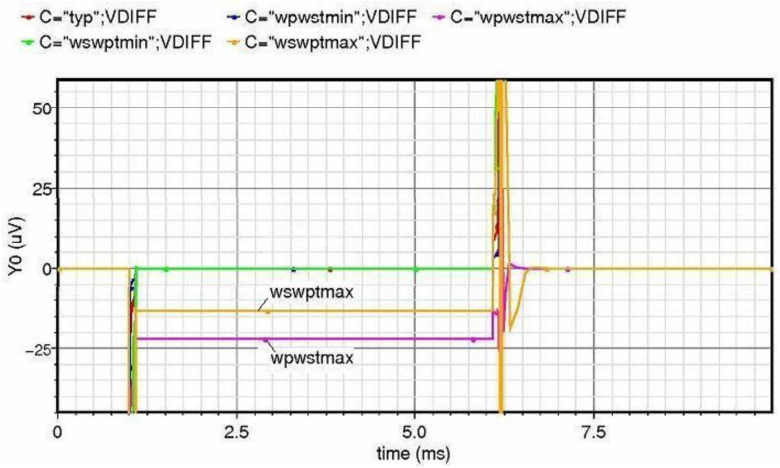

Figure 2.49: Worst cases of the voltage drop V_{diff}, transient analysis

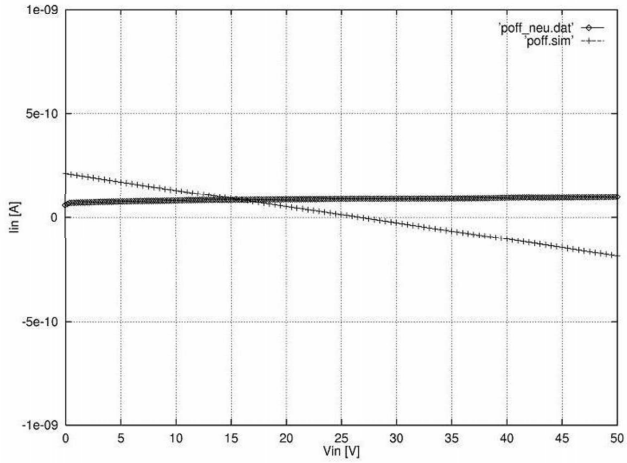

Figure 2.50: I_{in} as a function of V_{in}, OFF state, $\diamond$ measurement data, + simulation data

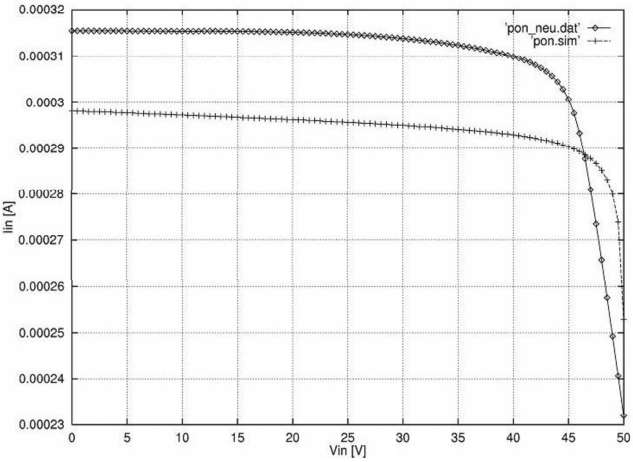

Figure 2.51: I_{in} as a function of V_{in}, ON state, $\diamond$ measurement data, + simulation data

The input current of the analog switch is shown in Fig. 2.50 and 2.51. On the one hand the current is nearly zero in the OFF state. On the other hand, in the ON state the current depends on the characteristics of the devices $T4 \ldots T7$ and $R2$.

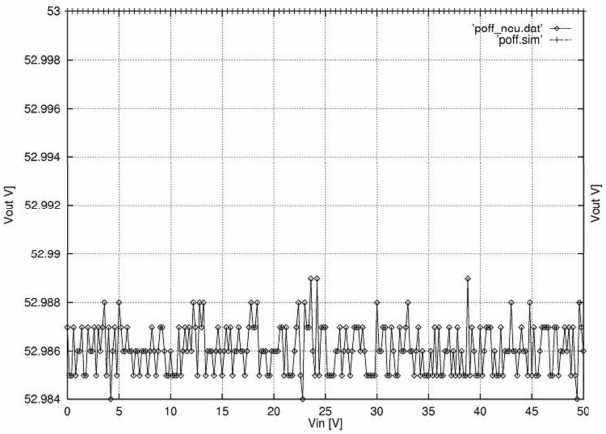

Figure 2.52: V_{out} as a function of V_{in}, OFF state, $\diamond$ measurement data, + simulation data

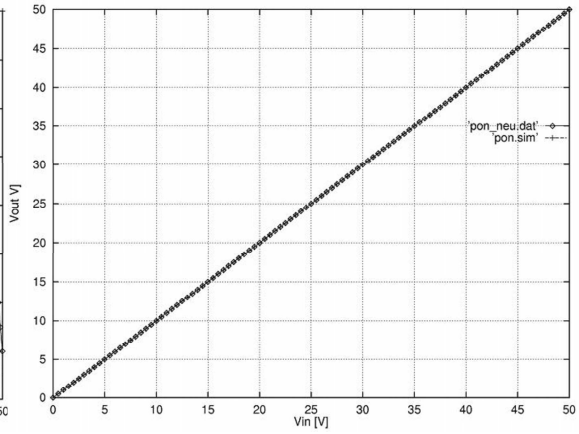

Figure 2.53: V_{out} as a function of V_{in}, ON state, $\diamond$ measurement data, + simulation data

The behaviour of the voltage on the output terminal depending on the input voltage is shown next. The output voltage V_{out} is nearly 53V in the OFF state illustrated in Fig. 2.52. V_{out} is not exactly 53V caused by several leakage currents in the circuit. In the ON state the output voltage follows the input voltage up to 50V. There is a minor deviation of V_{in} and V_{out}, the difference is shown in Fig. 2.54. The noise-like curve is caused on the one hand by the inaccuracy of the source unit and on the other hand by the inaccuracy of the measurement unit.

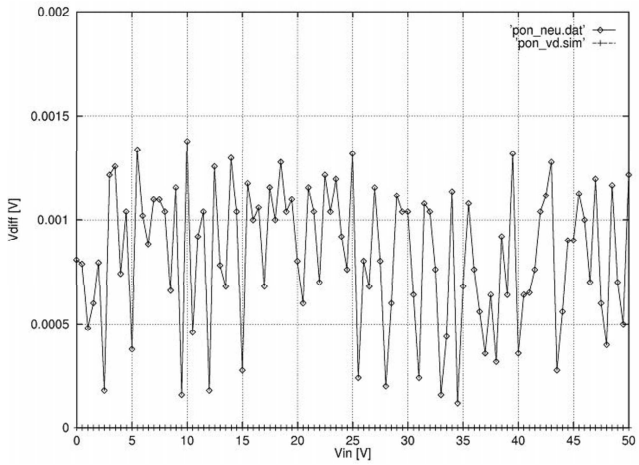

Figure 2.54: V_{diff} as a function of V_{in}, ON state, $\diamond$ measurement data, + simulation data

The whole circuit of the test macro for testing p-channel MOS transistors is shown in Fig. 2.55. On the left hand side is the 8-bit shift register which controls the ON/OFF state of the switch cascade. Further up there is the block for the generation of the voltage V_x. The digital block is connected with a bus-wire again for individual addressing of the analog switches on the right. To measure some important nodes of the switch-circuit an external switch is connected with additional contact pads (see Tab. 2.12 and Fig. 2.56). All other pads are identical with the pad assignment of Tab. 2.10.

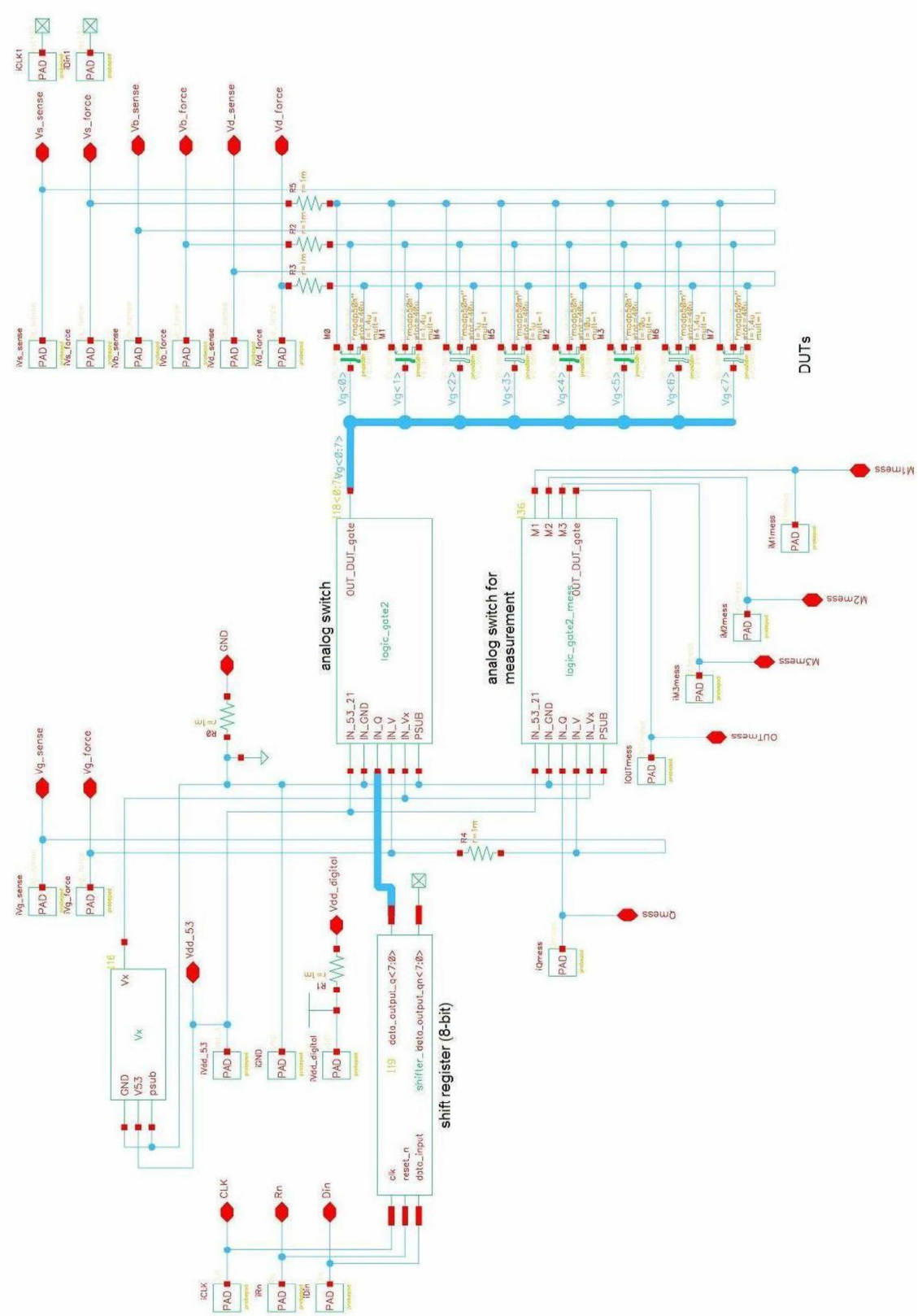

Figure 2.55: Schematic of the analog circuit design

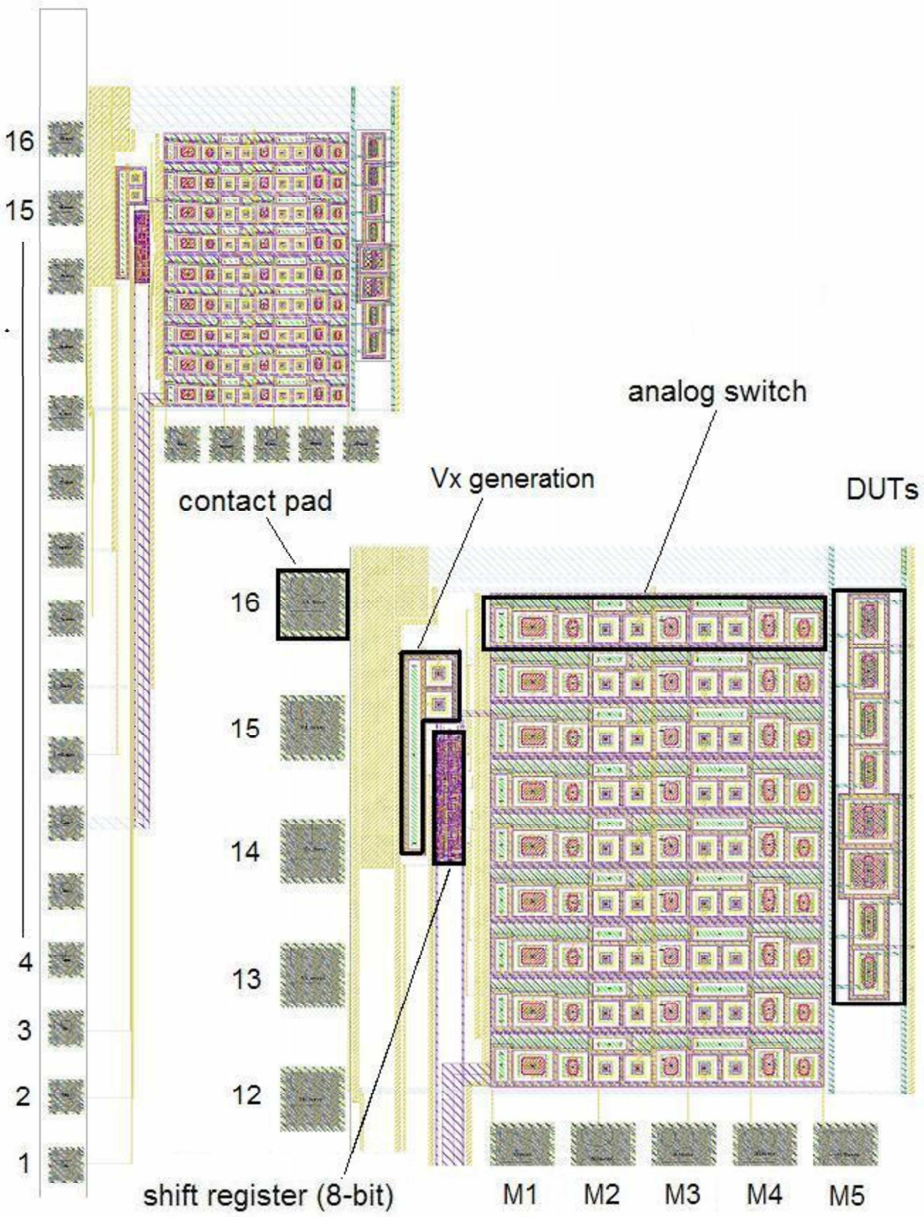

Figure 2.56: Layout of the analog circuit design

Table 2.12: Assignment of the measuring pads and the signals (Fig. 2.44)

Contact pad	M1	M2	M3	M4	M5
Signal	V_g	$V_{Gate_{T4}}$	$V_{Gate_{T7}}$	$V_{Gate_{T9}}$	V_{out}

Chapter 3

Layout and Guidelines

The previous chapter dealt with the structure and the design of the matrix test chip in detail. This chapter points out some important guidelines of the matrix test chip. First the layout of the whole design is shown. Additionally important facts are discussed which could limit the number of devices under test. Finally, several important layout-effects are described.

3.1 The layout

As illustrated in Fig. 3.1 the layout consists of previous described analog switch designs (2.6 and 2.7). The nMOS-switch-layout is shown in the bottom half, the pMOS-switch-layout is shown in the top half of the picture. Also a photo of the manufactured matrix test chip was made which is shown in Fig. 3.2.

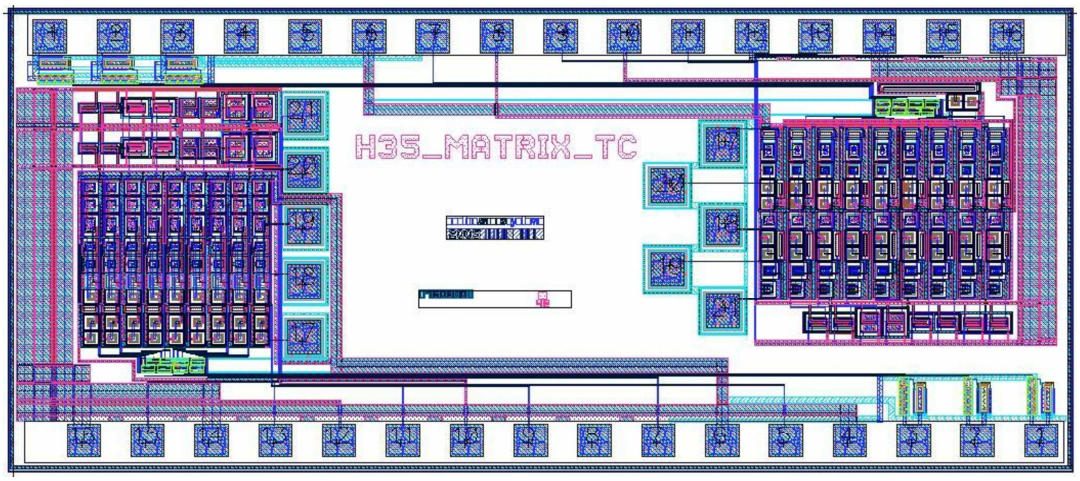

Figure 3.1: Layout of the matrix test chip

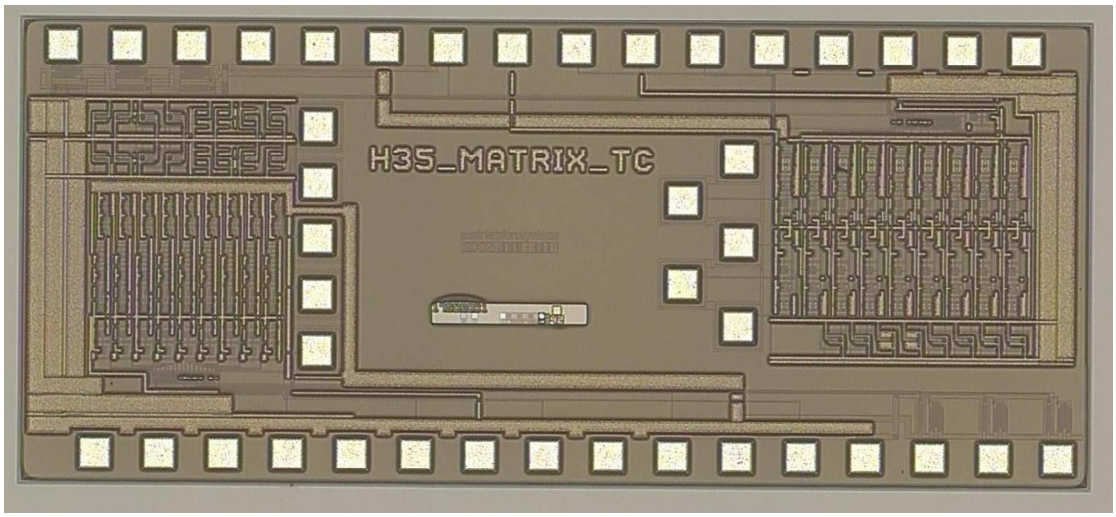

Figure 3.2: Photo of the matrix test chip

3.2 Substrate contacts

To ensure an efficient substrate contact between two High Voltage DNTUBs a proper spacing is indispensable. As described in [6] the channel for the holes moving to the substrate contacts is narrowed by the depletion-zones of two high voltage wells. To guarantee low resistances of the substrate-contact-resistors the spacing of two wells placed side by side must not be smaller than a certain defined value.

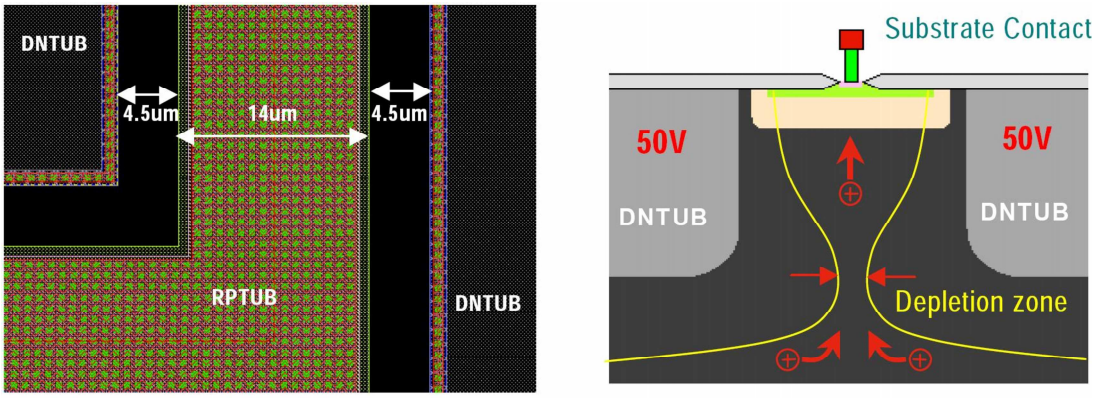

Figure 3.3: Spacing of two HV-DNTUBs with a substrate contact inside

3.3 Limitations of the test chip

The design of the test chip matrix can be extended to an arbitrary number of devices in the ideal case. In real the possible amount of devices under test has a limit. As shown in Fig. 3.4, the bulks of the DUTs of the nMOS-switch-design are all connected with the substrate which has the ground potential ($0V$,V_{SS}). During a measurement a drain-source current occurs which flows from the source unit $V_{D_{force}}$ to the source unit $V_{S_{force}}$.

This current I_S generates a voltage drop on the resistances $R_1 \ldots R_n$ of the metal-wire. The sense-node of the source-voltage V_S is normally adjusted to $0V$. It follows that the force-node of V_S has a lower potential than the sense-node. Measurements with large currents would cause large voltage drops. This indicates that the source-bulk-junction could become conductive.

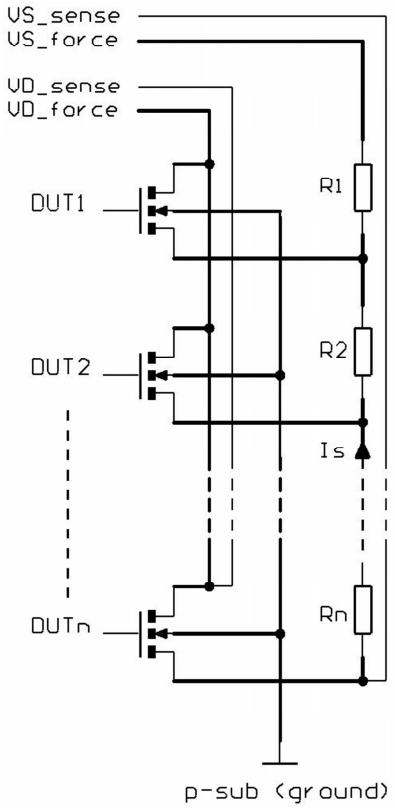

Figure 3.4: Placement of the DUTs, nMOS-test-macro

To avoid this problem some precautions against large voltage drops had to be performed:

- Devices with large current drive capabilities had to be placed at the top of the matrix
- The cross section of the source-force-wire had to be enlarged
- All kinds of metal layers had to be connected with interlayer connections to reduce the sheet resistance of the wire

Applying all considerations would yield lower resistances and lower voltage drops, respectively. The wires of the sense signals are all connected as close to the test devices as possible. This indicates that no unwanted resistances would be characterized.

Chapter 4

Automatized Device Measurement

Device measurement and DC characterization is very important to get accurate simulation models. This chapter deals with the principle of automated measurement. To achieve that aim special developed hardware and software is indispensable. Generally all devices must be analyzed separately. Therefore the individual elements are placed in so called scribe lines (SL) which areas cannot be used for product circuits. These areas provide structures for device testing and process monitoring. For analysis a highly modern measurement system is used to measure each device. This system normally consists of a probe cascade and a parameter analyzer. For analysis at least two probe needles have to be relocated for each element in the SL. This leads to the idea to switch the measurement signals of the PA automatically to the probe cascade, which means that you must place the wafer with the scribe lines only once.

4.1 Hardware

This section describes the hardware and its most important components.

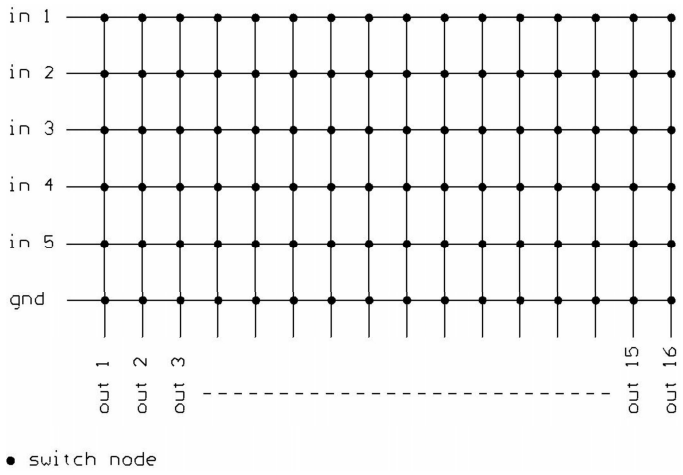

Figure 4.1: Principle of the switch matrix

The principle of the switch matrix is shown in Fig. 4.1. The input lines $in_1 \dots in_5$ are reserved for the signals of the source monitor units $SMU1 \dots SMU5$ of the parameter analyzer. The line *gnd* can be applied to connect the ground unit $GNDU$ of the PA for reference measurements. Each input line signal can be switched to one of the sixteen output terminals $out_1 \dots out_{16}$. The matrix consists of 6×16 switch nodes where each switch node consists of two analog switches. This is necessary to switch the force-part and the guard-part of the source-unit-signal (triax-connector).

The guidelines for the effective range of the forced current and the load voltage of the source-unit are

- Current range: 1nA ...1A
- Maximal load voltage: 100V

For the development some important characteristics of different types of switches (relays) were measured. The trouble was that generally manufacturers do not guarantee a switch function for contact currents below 1mA. Therefore some measurements had been performed before the development of the multiplexer-device started. Now the characteristic of the chosen relay type (DIP05-2A72-21L) are discussed in detail. The leakage current of the relay is shown in Fig. 4.2. It doesn't exceed a current-value of $10pA$. Deducing from that the relay has an isolation resistance of approximately $1T\Omega$.

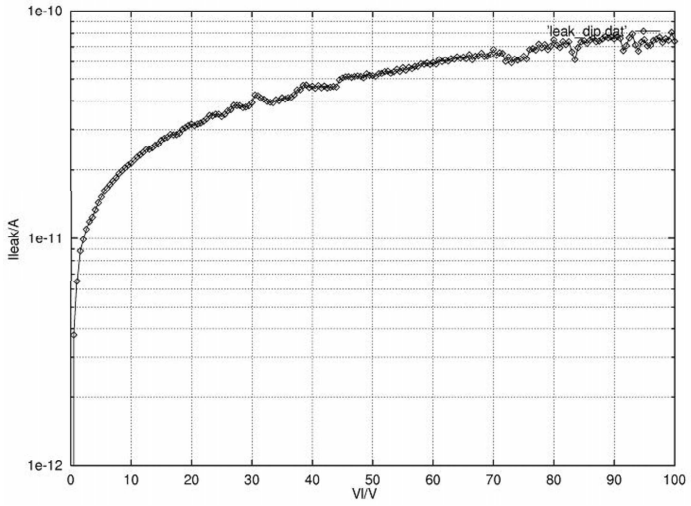

Figure 4.2: Off state leakage DIP05: leakage current Ileak/A vs. load voltage Vl/V

The resolution of the high-resolution-source-monitor-unit (HRSMU) is $100\mu V$. If forcing a current through the relay in the ON state the voltage drop on the contact resistance ($m\Omega$-range) is to small to measure it accurately. So, for measuring the characteristic of the relay in the ON state a series resistance R_x of $10M\Omega$ must connected in serial. The measurement circuit is shown in Fig. 4.3. As illustrated in Fig. 4.4 the current I_x through the switch is plotted as a function of the forced voltage V_x. This indicates that actually a signal current below $100pA$ can pass through the relay in the ON state.

The switch-mainframe provides a synchronous switching of 5 triax-input-signals to 16 triax-output-signals. Additionally, the outgoing triax-connections are connected in parallel to an IEEE-flat cable for an external probe card. This probe card is used to contact either a 16 pad standard SLM structure or the matrix test chip. To monitor the assignment of the input signals to the outgoing signals a led-array is implemented. The range of the signals which can be switched is $I_{DIP05} = 1nA$ to $1A$ and $V_{DIP05} = 100\mu V$ to $100V$.

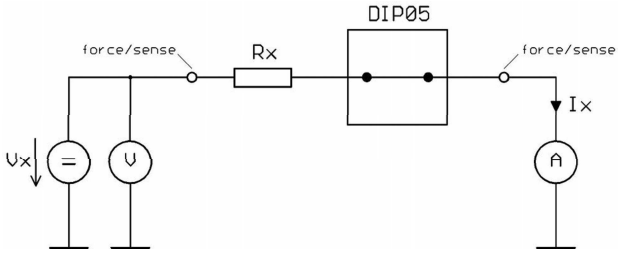

Figure 4.3: Measurement circuit, ON state

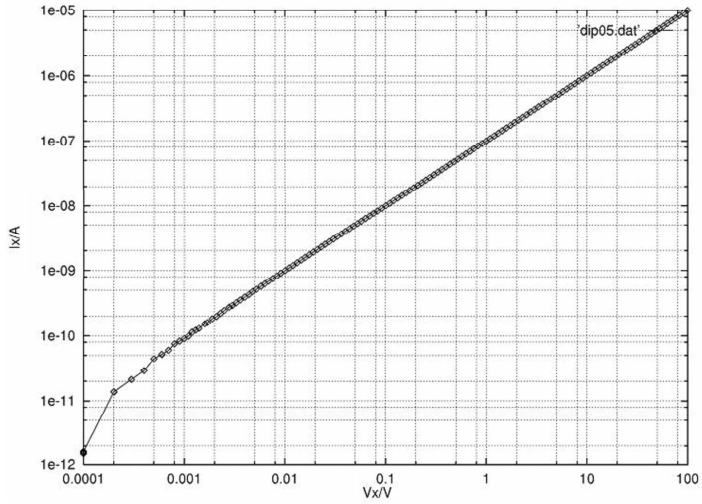

Figure 4.4: Characteristic of the series resistance R_x: I_x/A vs. V_x/V

4.1.1 Control unit

A micro controller (Risk processor, ATMEL) is used for controlling and communication. The control unit shown in Fig. 4.5 can be programmed either internally by a special console or externally by software. Further the matrix of the switch-mainframe can be programmed. Additionally, this unit allows the serial addressing of the control logic of the test chip (reset, clock, data).

4.1.2 Switch unit

The switch unit primarily consists of a switch matrix (6×16) which is controlled by the control unit. The schematic is shown in Fig. 4.6. Each switch-node is realized with a relay of type DIP05 to switch both, the signal itself and its guard. The relays are triggered with special cascaded power-shift-registers .

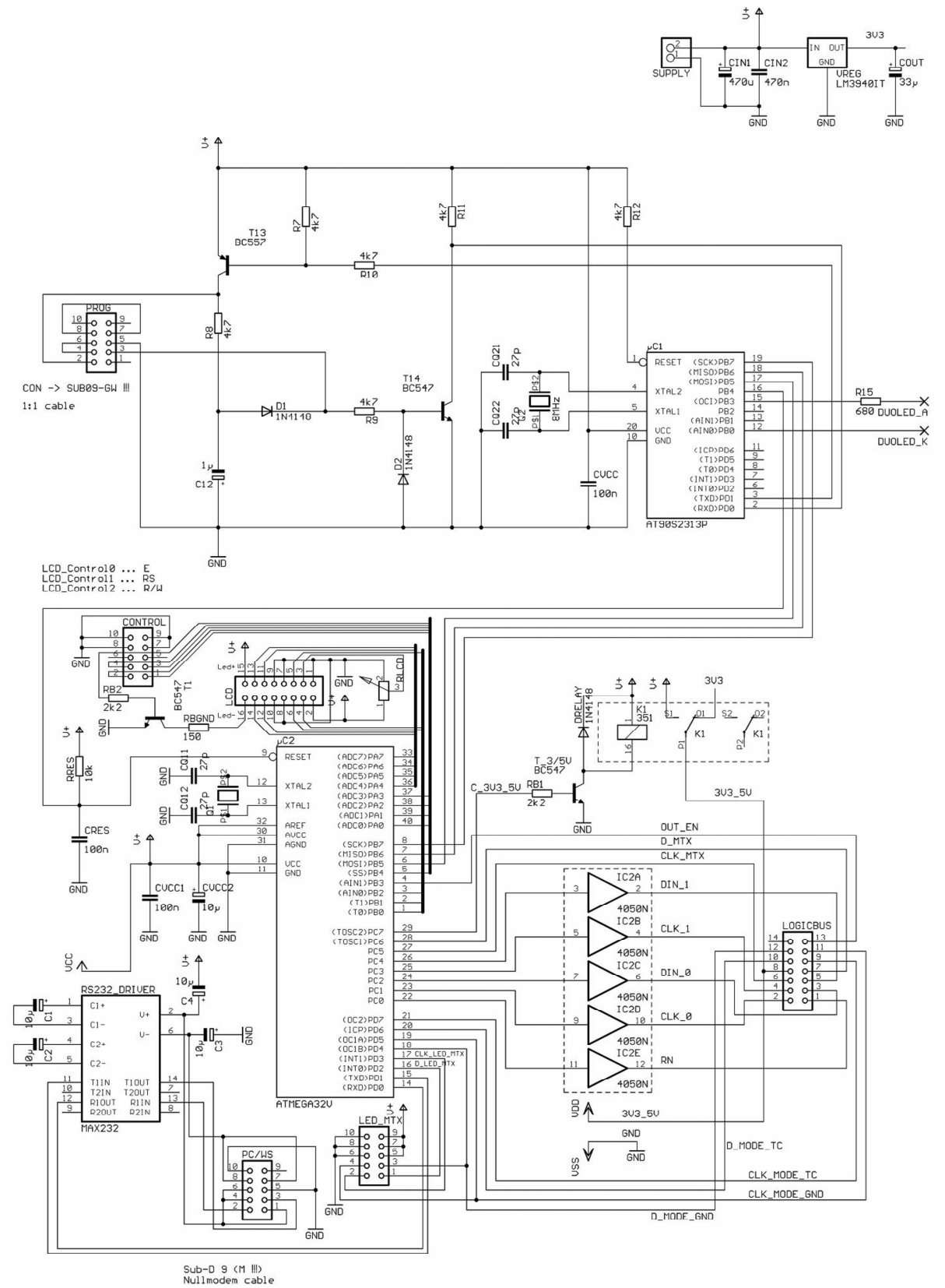

Figure 4.5: Schematic of the control unit

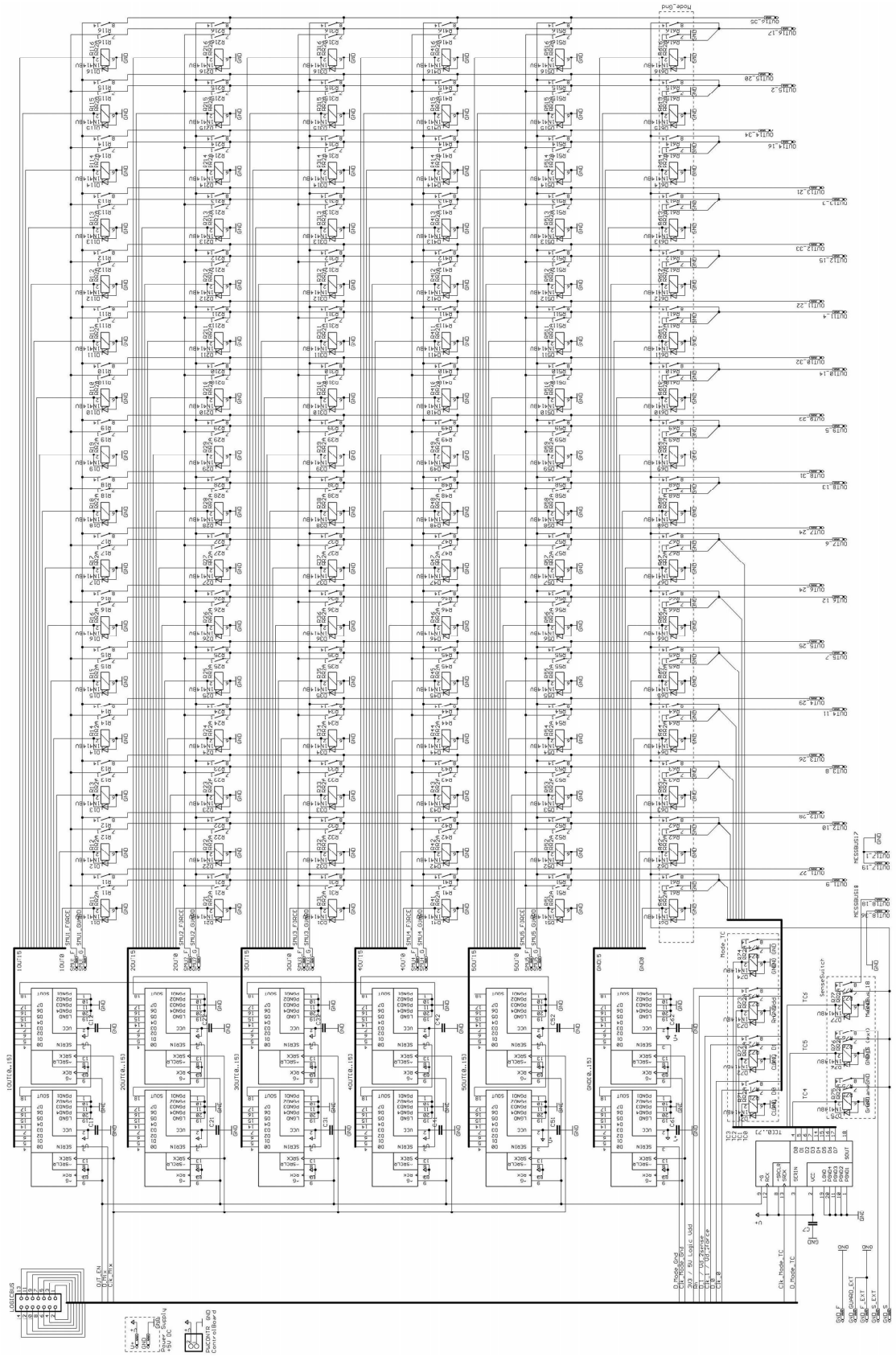

Figure 4.6: Schematic of the switch unit

4.2 Software

A further part of the work was the development of a measurement software which can be used in both, Windows and Unix operating systems. All skills like parameter setting, setup-file-creating, measuring in different modes, data reading and converting data-formats are implemented. Additionally the program is able to control the PA. Further, the software allows to control the switch-mainframe-matrix for automated measurements. Additionally, a measurement strategy is implemented to provide automated addressing of the matrix test chip. The software is written in *JAVA*, using the standard development kit *J2SDK* 1.4.2 and the development studio *NetBeans IDE* 4.1. A screenshot of the software is shown in Fig. 4.7.

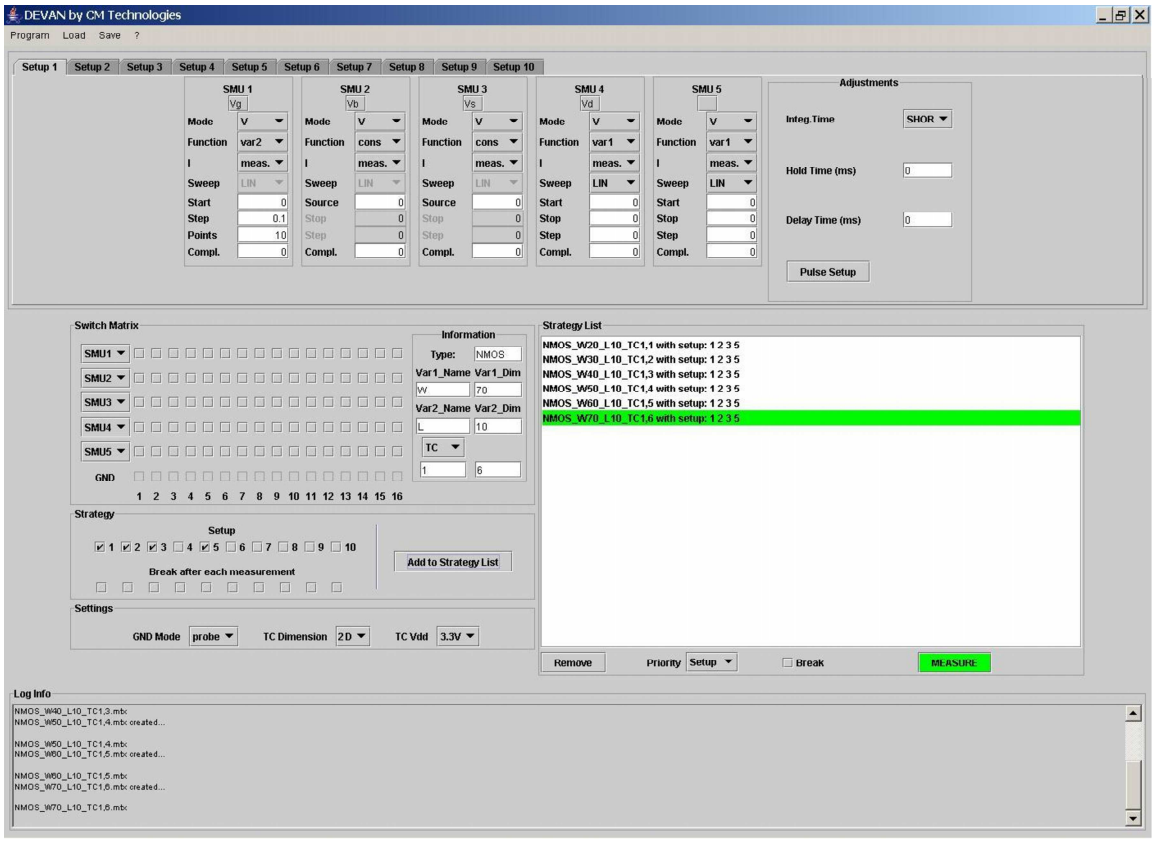

Figure 4.7: Screen shot of the software DEVAN

The program provides the creation, loading and storing of 10 setup-files. Each setup-file contains a complete adjustment of all SMUs needed for one measurement sequence. In addition, the switch matrix can be set either for matrix test chip or for normal scribe line measurements. Additional settings are implemented for the test chip. All settings are added in the strategy list which is automatically executed step by step. The advantage of this software is the easy handling and the symbolic language, for example the measurement settings can be created with *unix* scripts or similar tools.

A detailed description of the software can be found in the documentation [3].

Chapter 5

Outlook

The semiconductor industry intends to design more precise circuits to increase the stability and to maximize the effectiveness. Therefore, the characterization of semiconductor devices is a very important process. Especially the modeling of different electrical behaviour of devices due to process parameter gradients is indispensable for the design of precise applications.

Enhanced mismatch modeling needs large test structures and an enormous effort to acquire data for statistical analysis. The improved concept of measurement presented in this thesis allows a fast and accurate analysis of many devices. This measurement method enables the analysis of short distance mismatch, long distance mismatch and pair mismatch by using one structure. The very good results of the test chip evaluation leads to the design of the new test chip 'Matrix Reloaded' which contains 5400 devices for characterization. Pictures of the test chip are shown in Fig. 5.1 and Fig. 5.2.

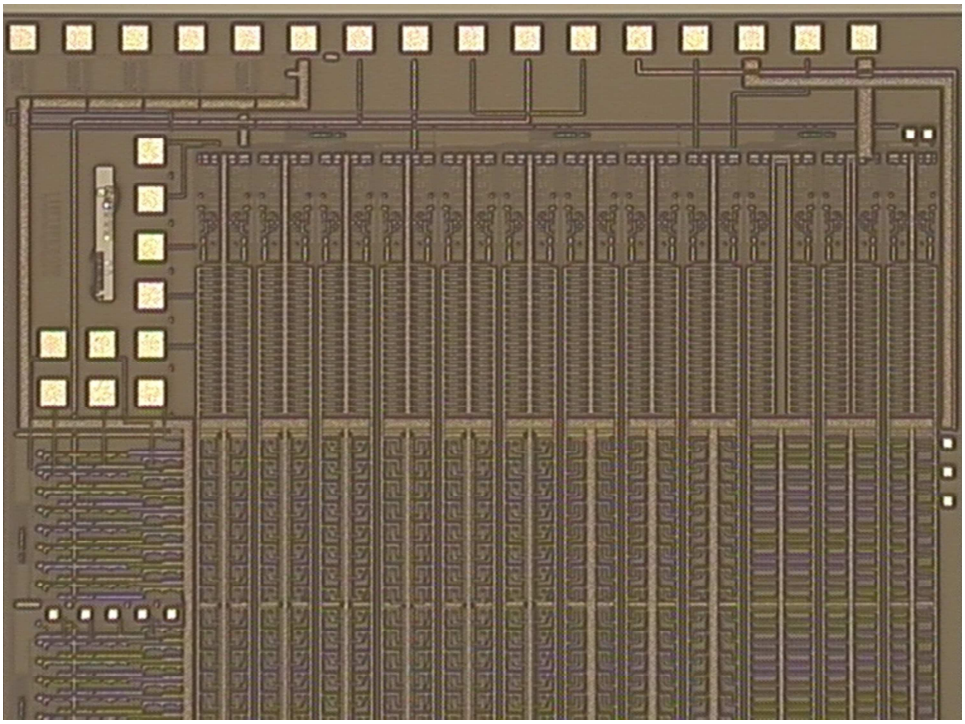

Figure 5.1: Picture 1 of the test chip 'Matrix Reloaded'

The design of this test macro was not included in this thesis in order to avoid going beyond the scope. The plans for the future contain a precise characterization of the new test chip, the extraction of various statistical parameters and the interpretation of the results. The goal is to describe the mismatch behaviour depending on parameters like the spatial distance between two devices, process parameter gradients, temperature, etc. All this influences have to be taken into account to guarantee a good mixed signal circuit performance.

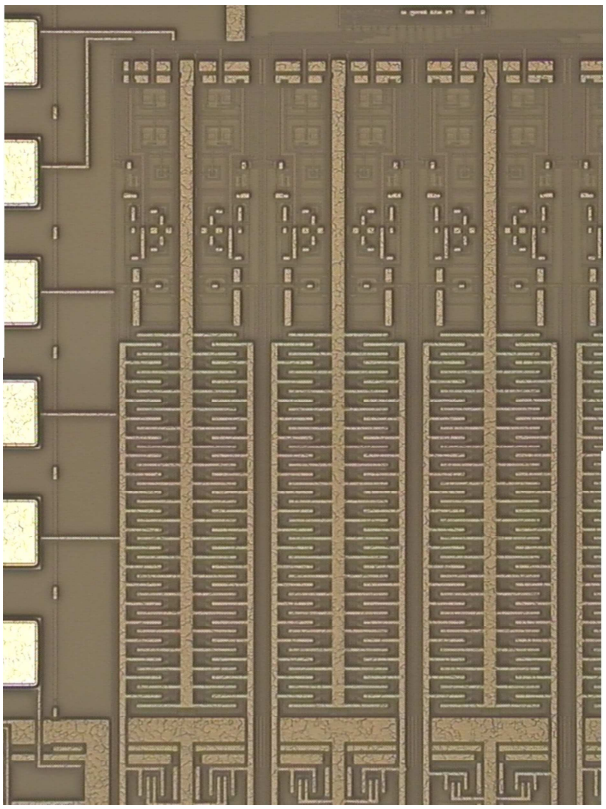

Figure 5.2: Picture 2 of the test chip 'Matrix Reloaded'

Chapter 6

Conclusion

In this thesis design and simulation of a mixed signal test chip for highly accurate DC measurements were presented. First a brief introduction was given on the most important applications of the MOSFET where the MOSFET-switch, the transmission gate and the constant current source were discussed in detail.

The main focus of the thesis was the design of a test chip which enables automated measurements for high voltage nMOS transistors and high voltage pMOS transistors. Therefore a matrix structure was investigated to provide an ideal test behaviour and to reduce space requirements.

First the design of the transmission gate for nMOS transistors was developed. Simulations were performed and several problems due to high operating voltages and unwanted resistance effects were solved. Then the whole chip including the digital control logic, the high-voltage n-transmission gates and the devices under test was designed.

Subsequently the transmission gate for pMOS transistors was developed and simulations were made. Especially the range of the operating voltages of the pMOS transistor was considered. Since the design is more complex, mainly problems due to the influence of process variation were solved. In the next step an entire chip including the digital control logic, the high-voltage p-transmission gates and the devices under test was designed.

Finally, measurements were performed on both test structures and very good agreement with the simulation data was found. Moreover, a switch mainframe which additionally provides signals to control the test chip was developed and an operating system independent measurement software which offers the addressing for automated measurement was implemented.

The development of the test chip matrix enables more accurate and less time consuming device measurements which can be performed automatically.

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